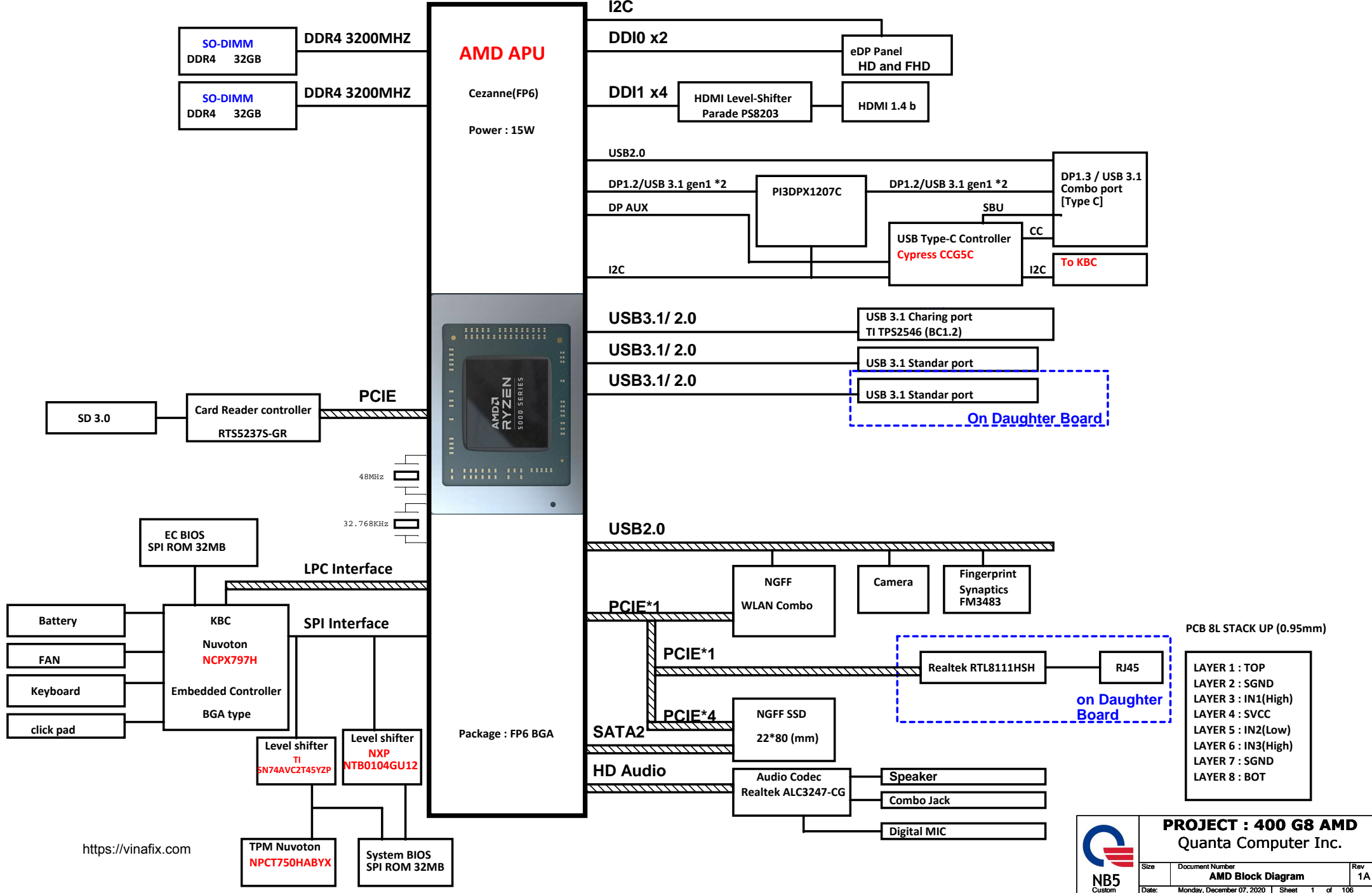
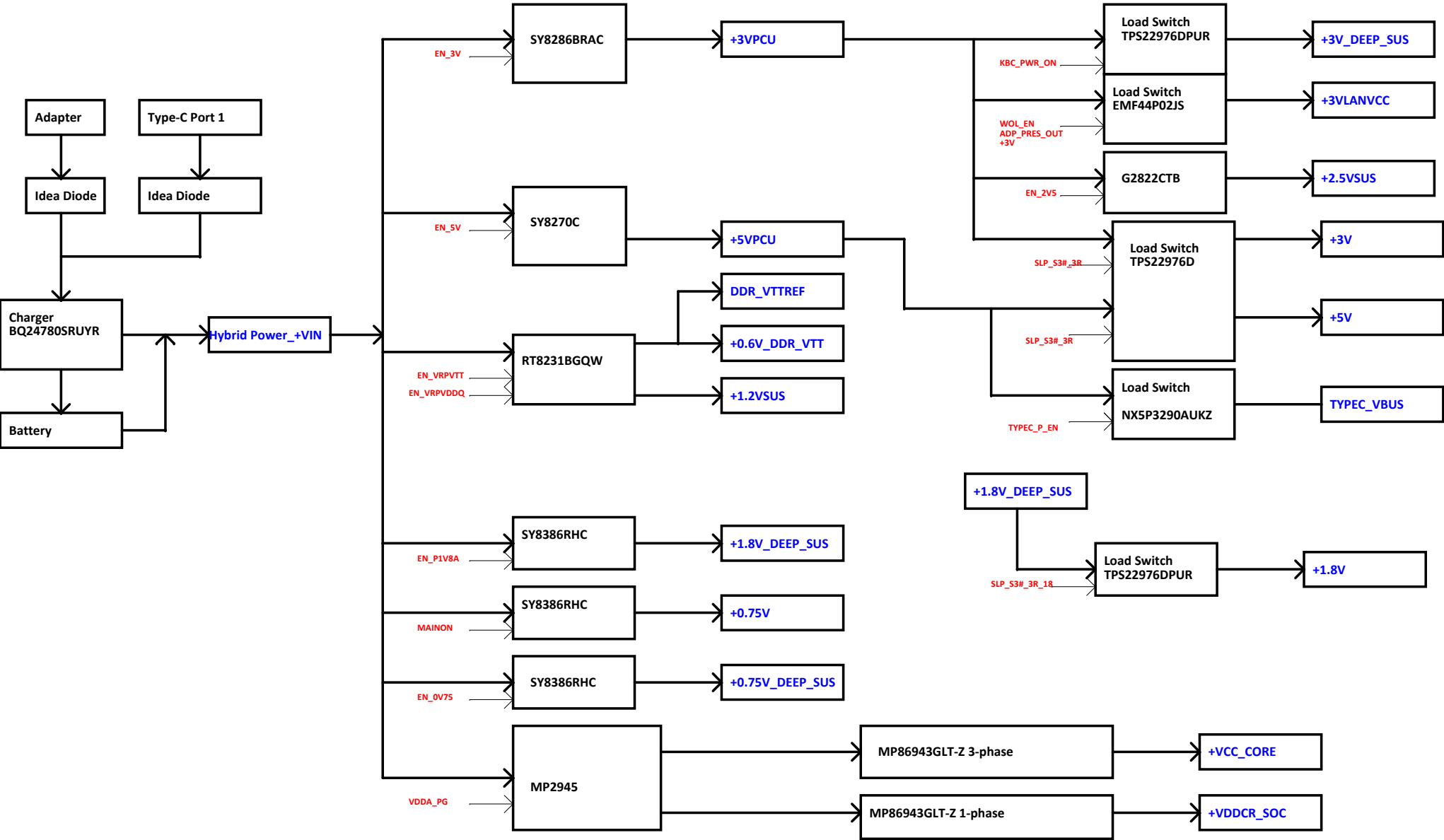


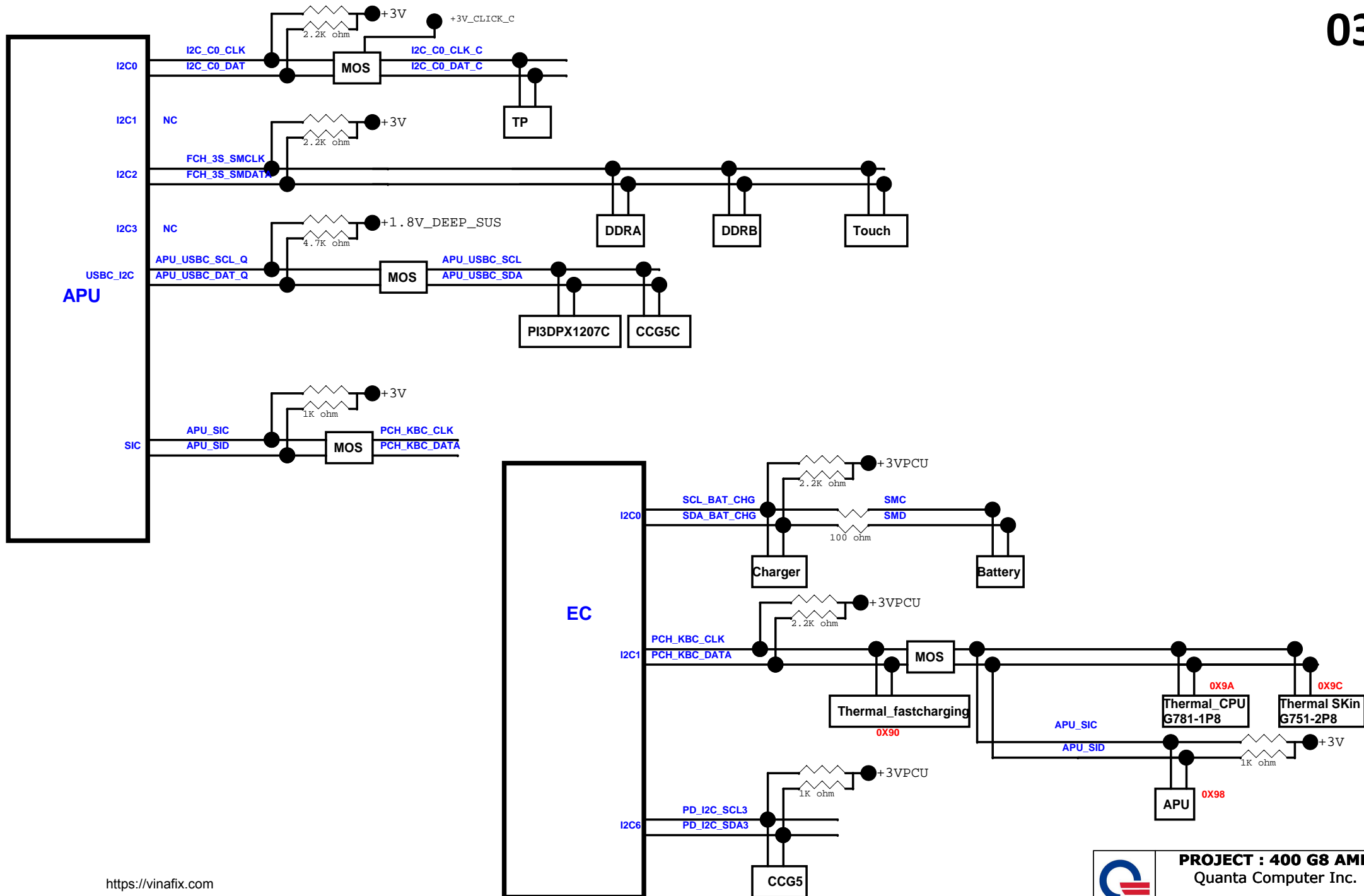
# 400s G8 14"/15" AMD Cezanne UMA



# POWER BLOCK DIAGRAM

02

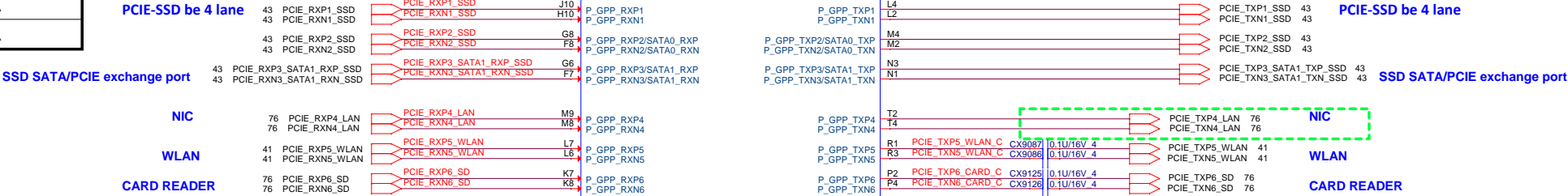


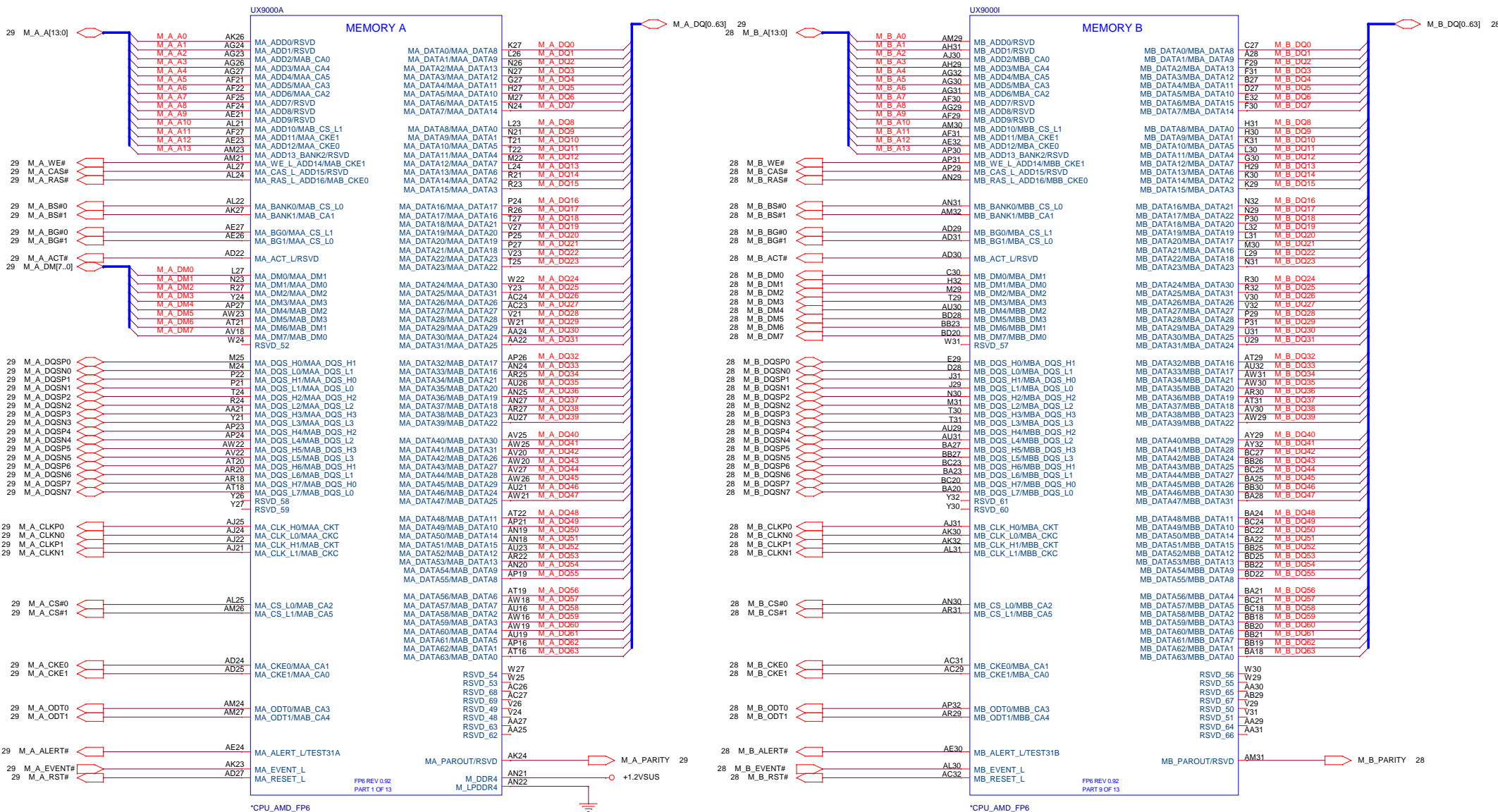


APU PCIE

AMD APU	TOP BSQ	QBCON

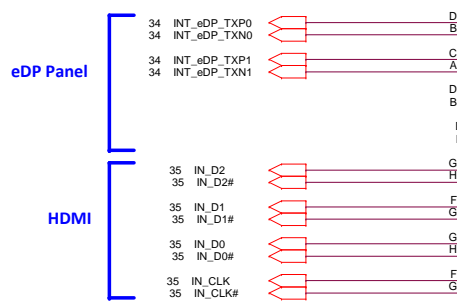
PCIE Port	Function
PCIE_0	SSD_PCIE
PCIE_1	SSD_PCIE
PCIE_2	SSD_PCIE
PCIE_3	SSD_PCIE/SATA
PCIE_4	NIC
PCIE_5	WLAN
PCIE_6	Care Reader
PCIE_7	NA
PCIE_8	NA





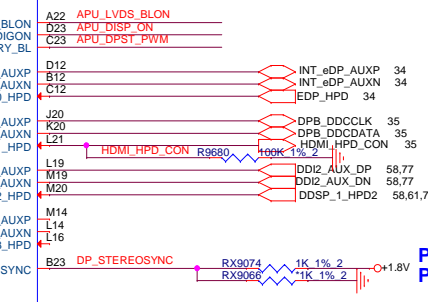
# APU DISPLAY and MISC

06



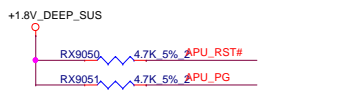
UX9000C

## DISPLAY/SVI2/JTAG/TEST



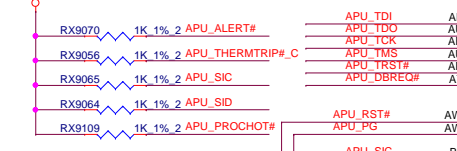
**eDP**  
**HDMI**  
**TypeC**

**PU For internal PD For customer**

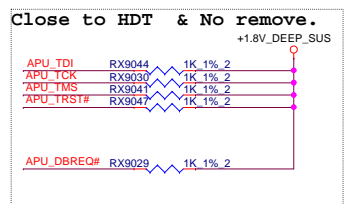


**ESD mount**

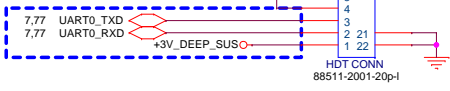
**2018/12/12 PV STAGE**  
**stuff CX9066/CX9067 to solve ESD issue**



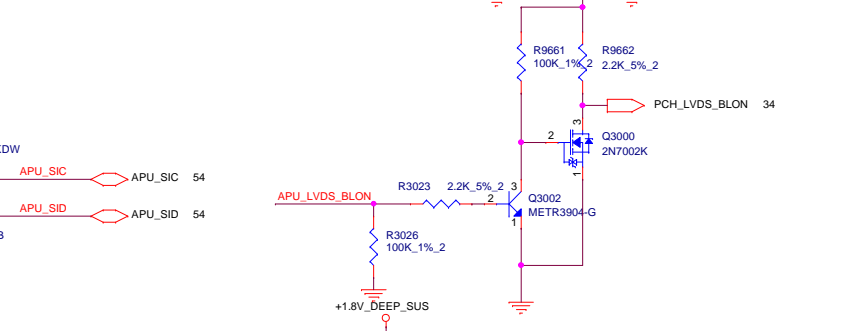
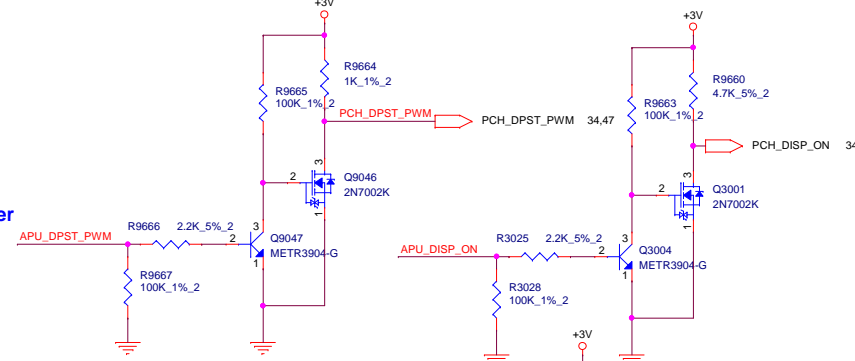
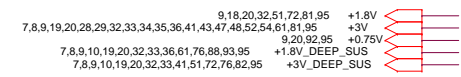
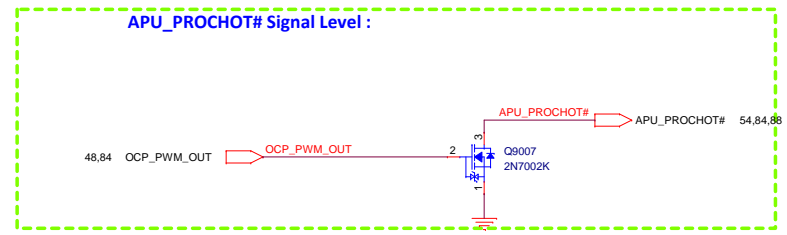
**HDT+ Connector for Debug only**



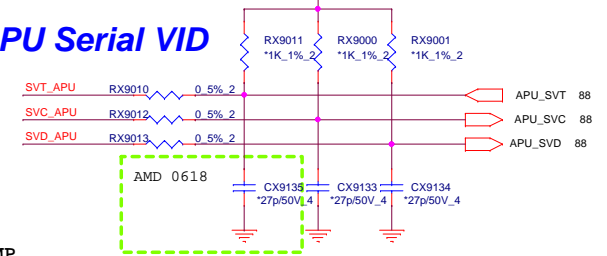
**400 G7**



**APU\_PROCHOT# Signal Level :**



**APU Serial VID**



**Boot-VID code**

SVC	SVD	VOLTAGE
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

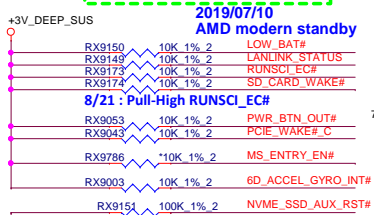
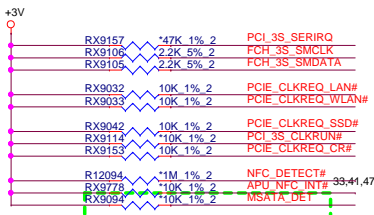
**PROJECT : 400 G8 AMD**  
**Quanta Computer Inc.**



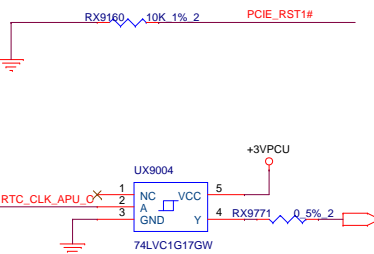
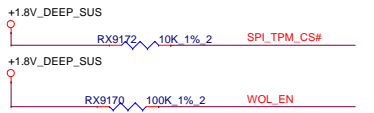
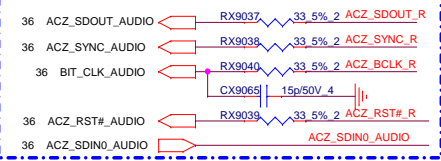
Size	Document Number	RR 3/7(DIS/MISC)	Rev 1A
Date: Monday, December 07, 2020	Sheet	6	of 106

<https://vinafix.com>

# APU GPIO/AZ/UART

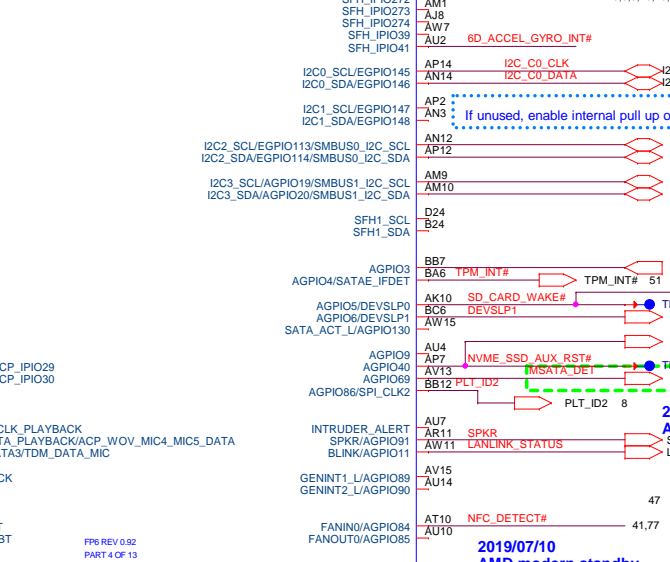


## HDA INTERFACE



<https://vinafix.com>

## ACPI/AUDIO/I2C/GPIO/MISC



FP6 REV 0.92 PART 4 OF 13

\*CPU\_AMD\_FP6

UX9000E

CLK/LPC/EMMC/SD/SPI/eSPI/UART

CLK\_REQ0\_L/SATA\_ISO\_L/SATA\_ZP0\_L/AGPIO92

CLK\_REQ1\_L/AGPIO115

CLK\_REQ2\_L/AGPIO116

CLK\_REQ3\_L/SATA\_IS1\_L/SATA\_ZP1\_L/AGPIO131

CLK\_REQ4\_L/OSCIN/EGPIO132

CLK\_REQ5\_L/EGPIO120

CLK\_REQ6\_L/EGPIO121

CLK\_REQ7\_L/AGPIO122

CLK\_REQ8\_L/AGPIO123

CLK\_REQ9\_L/AGPIO124

CLK\_REQ10\_L/AGPIO125

CLK\_REQ11\_L/AGPIO126

CLK\_REQ12\_L/AGPIO127

CLK\_REQ13\_L/AGPIO128

CLK\_REQ14\_L/AGPIO129

CLK\_REQ15\_L/AGPIO130

CLK\_REQ16\_L/AGPIO131

CLK\_REQ17\_L/AGPIO132

CLK\_REQ18\_L/AGPIO133

CLK\_REQ19\_L/AGPIO134

CLK\_REQ20\_L/AGPIO135

CLK\_REQ21\_L/AGPIO136

CLK\_REQ22\_L/AGPIO137

CLK\_REQ23\_L/AGPIO138

CLK\_REQ24\_L/AGPIO139

CLK\_REQ25\_L/AGPIO140

CLK\_REQ26\_L/AGPIO141

CLK\_REQ27\_L/AGPIO142

CLK\_REQ28\_L/AGPIO143

CLK\_REQ29\_L/AGPIO144

CLK\_REQ30\_L/AGPIO145

CLK\_REQ31\_L/AGPIO146

CLK\_REQ32\_L/AGPIO147

CLK\_REQ33\_L/AGPIO148

CLK\_REQ34\_L/AGPIO149

CLK\_REQ35\_L/AGPIO150

CLK\_REQ36\_L/AGPIO151

CLK\_REQ37\_L/AGPIO152

CLK\_REQ38\_L/AGPIO153

CLK\_REQ39\_L/AGPIO154

CLK\_REQ40\_L/AGPIO155

CLK\_REQ41\_L/AGPIO156

CLK\_REQ42\_L/AGPIO157

CLK\_REQ43\_L/AGPIO158

CLK\_REQ44\_L/AGPIO159

CLK\_REQ45\_L/AGPIO160

CLK\_REQ46\_L/AGPIO161

CLK\_REQ47\_L/AGPIO162

CLK\_REQ48\_L/AGPIO163

CLK\_REQ49\_L/AGPIO164

CLK\_REQ50\_L/AGPIO165

CLK\_REQ51\_L/AGPIO166

CLK\_REQ52\_L/AGPIO167

CLK\_REQ53\_L/AGPIO168

CLK\_REQ54\_L/AGPIO169

CLK\_REQ55\_L/AGPIO170

CLK\_REQ56\_L/AGPIO171

CLK\_REQ57\_L/AGPIO172

CLK\_REQ58\_L/AGPIO173

CLK\_REQ59\_L/AGPIO174

CLK\_REQ60\_L/AGPIO175

CLK\_REQ61\_L/AGPIO176

CLK\_REQ62\_L/AGPIO177

CLK\_REQ63\_L/AGPIO178

CLK\_REQ64\_L/AGPIO179

CLK\_REQ65\_L/AGPIO180

CLK\_REQ66\_L/AGPIO181

CLK\_REQ67\_L/AGPIO182

CLK\_REQ68\_L/AGPIO183

CLK\_REQ69\_L/AGPIO184

CLK\_REQ70\_L/AGPIO185

CLK\_REQ71\_L/AGPIO186

CLK\_REQ72\_L/AGPIO187

CLK\_REQ73\_L/AGPIO188

CLK\_REQ74\_L/AGPIO189

CLK\_REQ75\_L/AGPIO190

CLK\_REQ76\_L/AGPIO191

CLK\_REQ77\_L/AGPIO192

CLK\_REQ78\_L/AGPIO193

CLK\_REQ79\_L/AGPIO194

CLK\_REQ80\_L/AGPIO195

CLK\_REQ81\_L/AGPIO196

CLK\_REQ82\_L/AGPIO197

CLK\_REQ83\_L/AGPIO198

CLK\_REQ84\_L/AGPIO199

CLK\_REQ85\_L/AGPIO200

CLK\_REQ86\_L/AGPIO201

CLK\_REQ87\_L/AGPIO202

CLK\_REQ88\_L/AGPIO203

CLK\_REQ89\_L/AGPIO204

CLK\_REQ90\_L/AGPIO205

CLK\_REQ91\_L/AGPIO206

CLK\_REQ92\_L/AGPIO207

CLK\_REQ93\_L/AGPIO208

CLK\_REQ94\_L/AGPIO209

CLK\_REQ95\_L/AGPIO210

CLK\_REQ96\_L/AGPIO211

CLK\_REQ97\_L/AGPIO212

CLK\_REQ98\_L/AGPIO213

CLK\_REQ99\_L/AGPIO214

CLK\_REQ100\_L/AGPIO215

CLK\_REQ101\_L



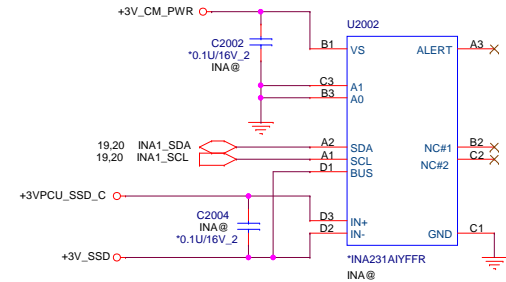




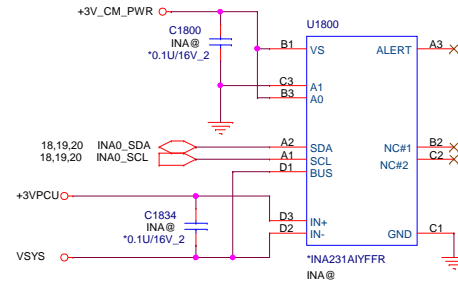




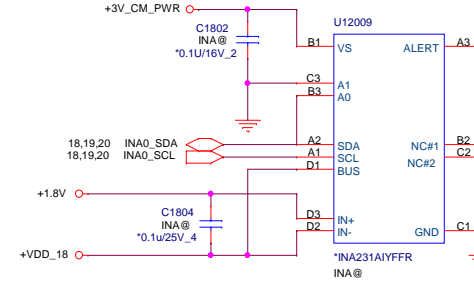
**SSD Placed Close to R4300**



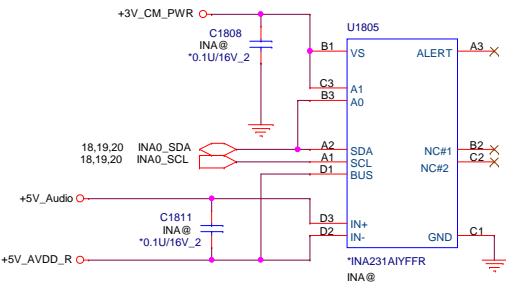
**CCG5C Placed Close to R6109**



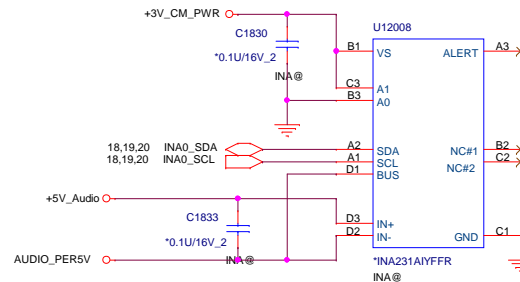
**CPU\_+VDD\_18 Placed Close to RX9046**



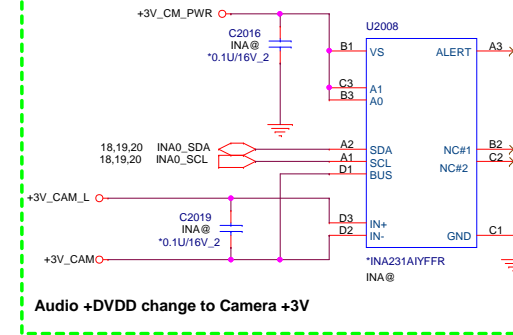
**CODEC Placed Close to R3604**



**CODEC Placed Close to L3601**

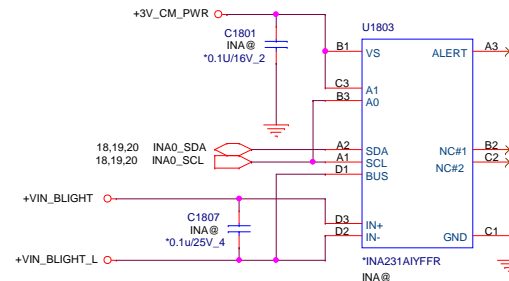


**Camera Placed Close to R3412**

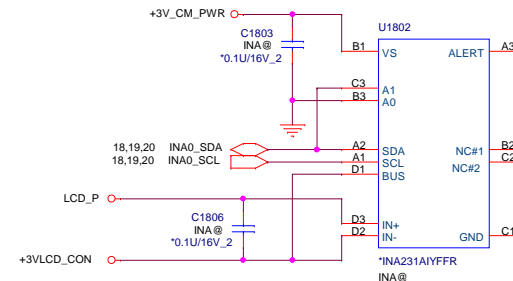


Audio +DVDD change to Camera +3V

**LCD BL Placed Close to R3415**



**CO-LAY WITH L3400 LCD T-CON**



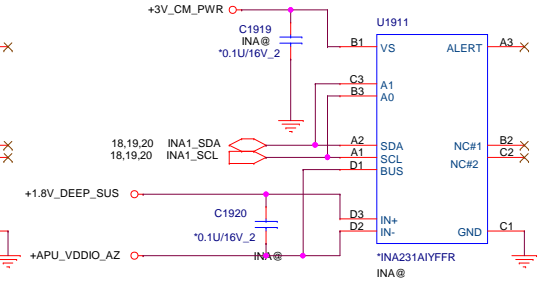
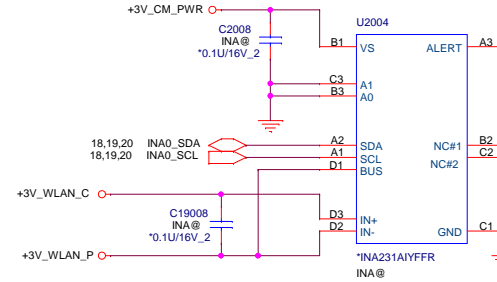
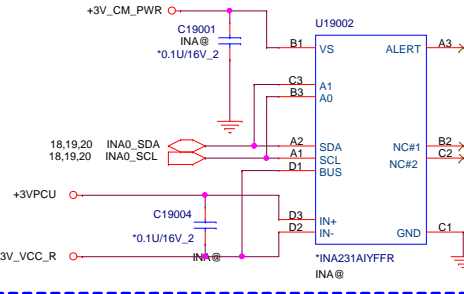
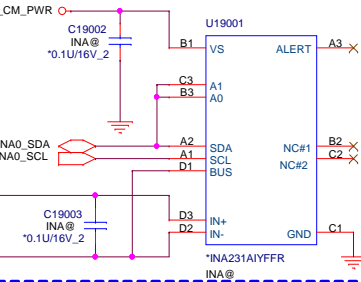
Audio +DVDD change NA  
<https://vinafix.com>

EC CO-LAY WITH L4703

EC CO-LAY WITH L4702

WLAN Place close to R4101

+APU\_VDDIO\_AZ CO-LAY WITH RX9058

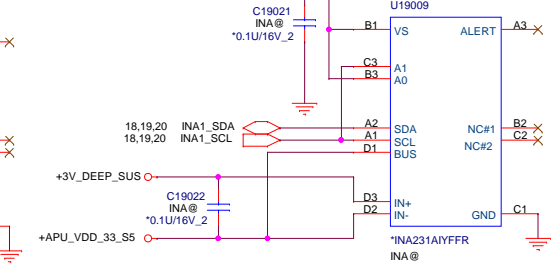
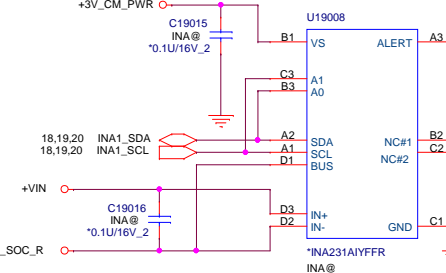
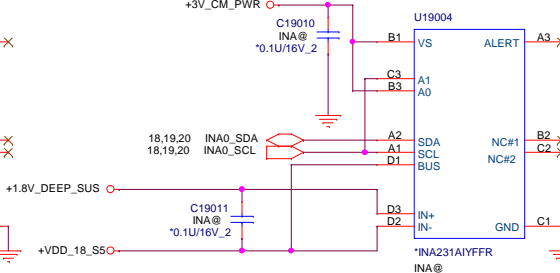
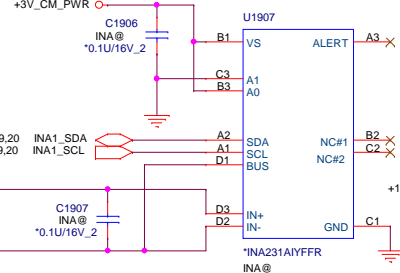


+APU\_VDD\_33 Place close to RX9055

+VDD\_18\_S5 Place close to RX9049

+VIN\_VDDCR\_SOC Close PR9000

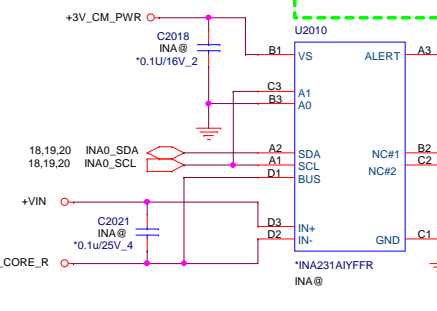
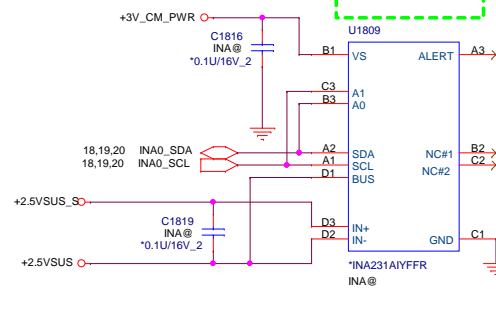
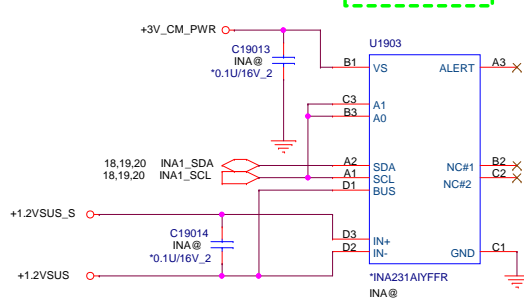
+APU\_VDD\_33\_S5 Place close to RX9057



+1.2VSUS CLOSE PR8706

+2.5VSUS CLOSE PR8717

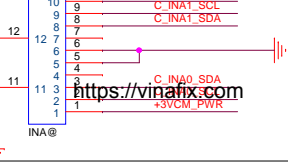
+VIN\_VCC\_CORE CLOSE PR8900



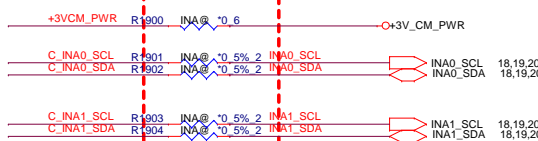
Close HDT9000

\*Current monitor conn.

CON1900

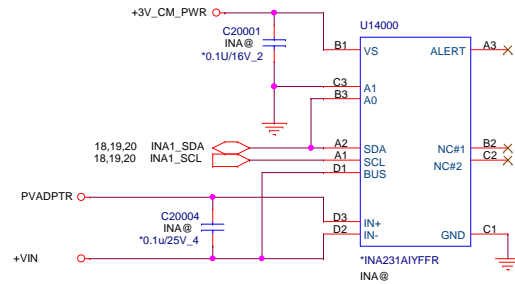


Stuff in Monitor side



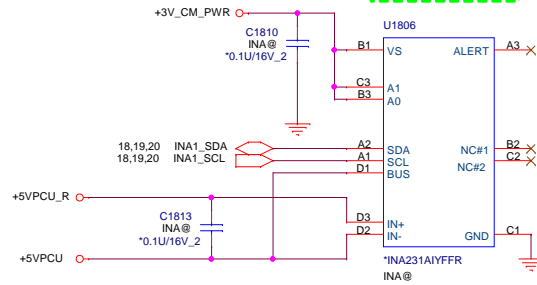
+VIN\_ADP

CLOSE PR8200



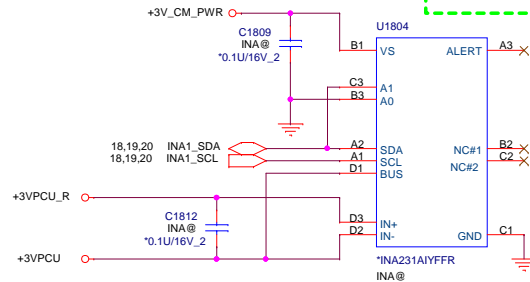
+5VPCU

CLOSE PR8623



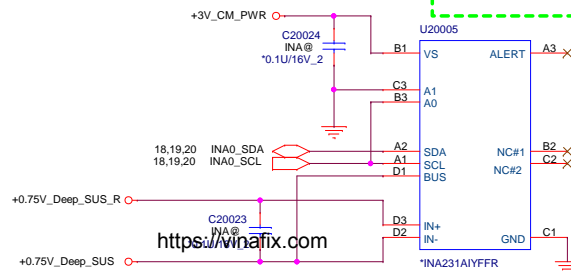
+3VPCU

CLOSE PR8622



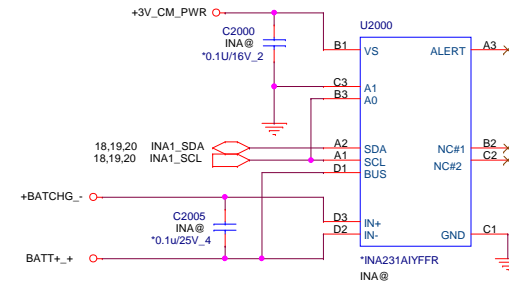
+0.75V\_Deep\_SUS

CLOSE PR9213



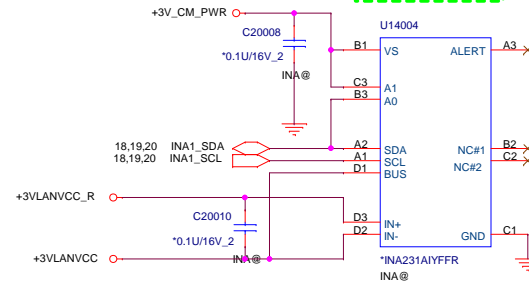
Battery

CLOSE PL8400



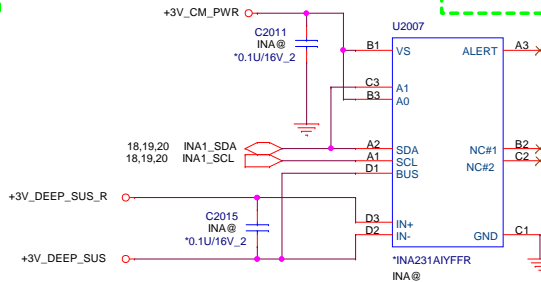
+3VLAVCC

CLOSE PR9525



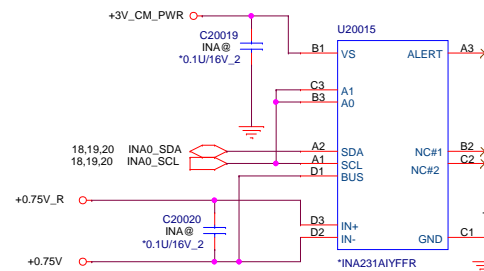
+3V\_Deep\_SUS

CLOSE PR9503



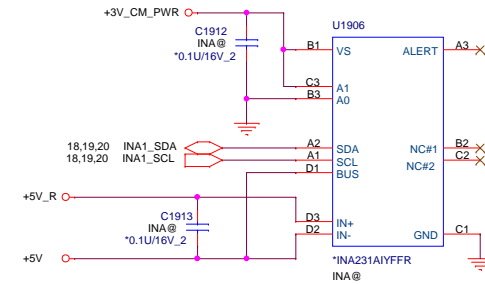
+0.75V

CLOSE PR9201



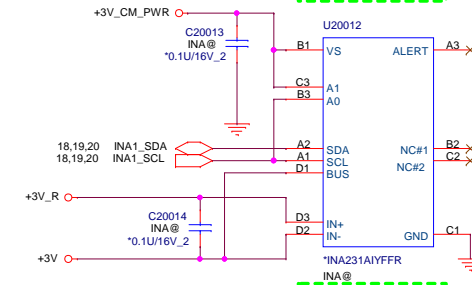
+5V

CLOSE PR9502



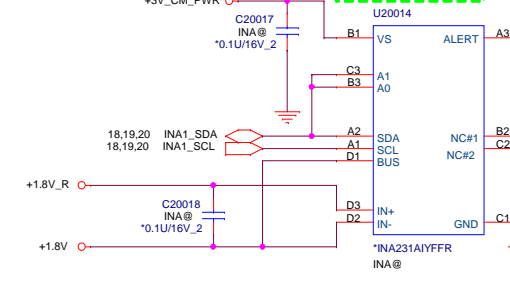
+3V

CLOSE PR9509



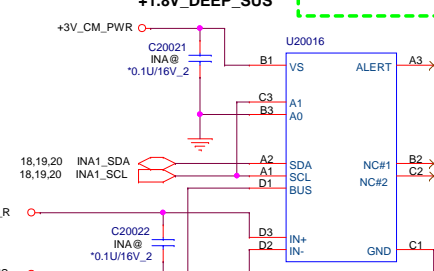
+1.8V

CLOSE PR9510



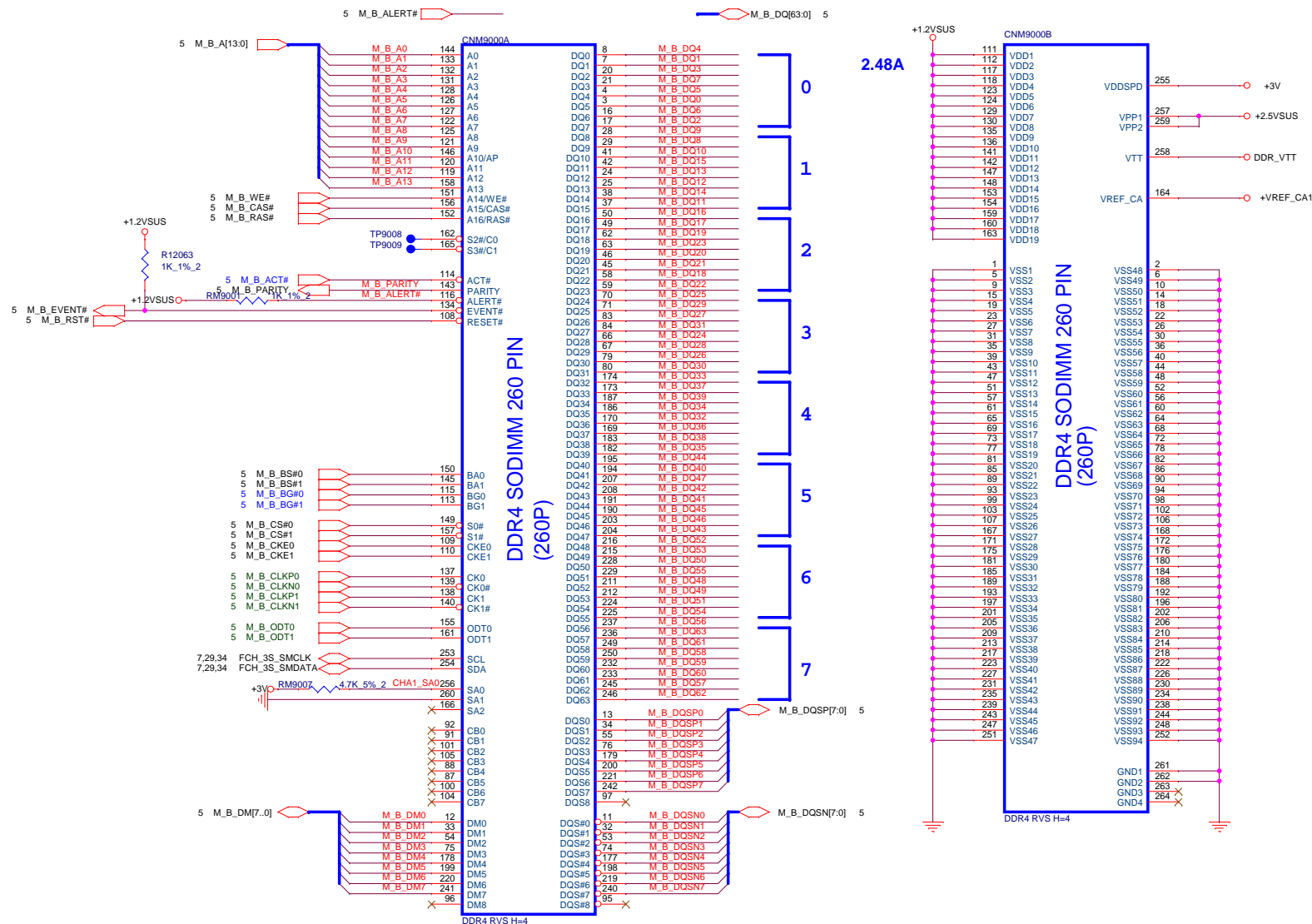
+1.8V\_Deep\_SUS

CLOSE PR9301

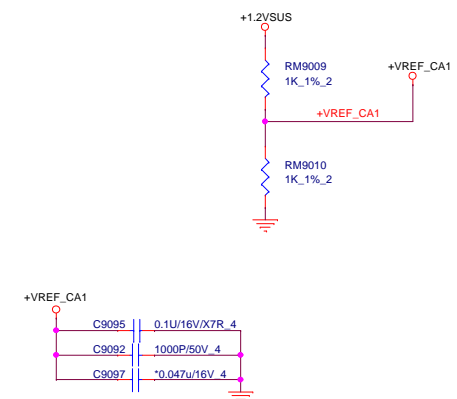


**PROJECT : 400 G8 AMD**  
**Quanta Computer Inc.**

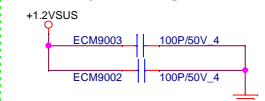
Size Custom	Document Number <b>CURRENT SENSOR-3</b>	Rev 1A
Date: Monday, December 07, 2020		Sheet 0 of 106

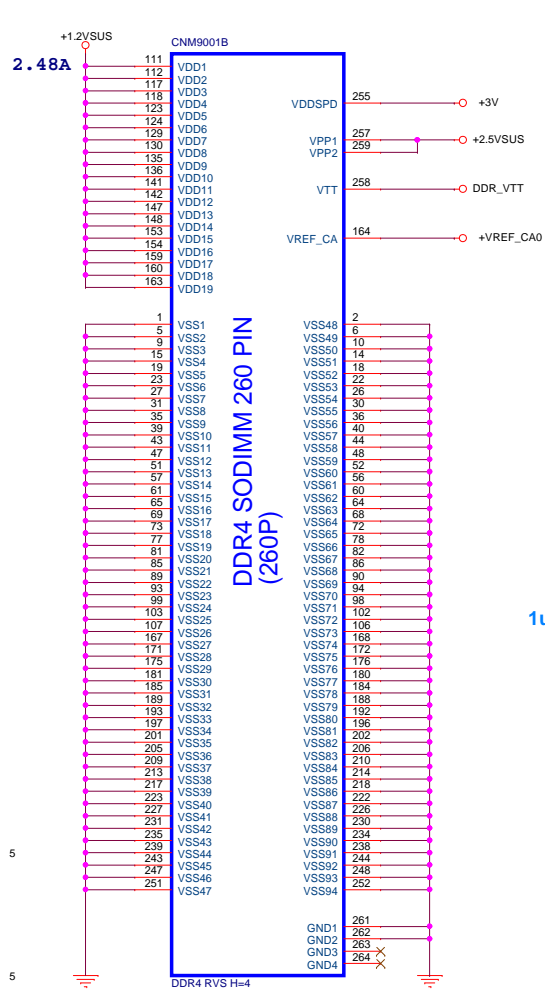
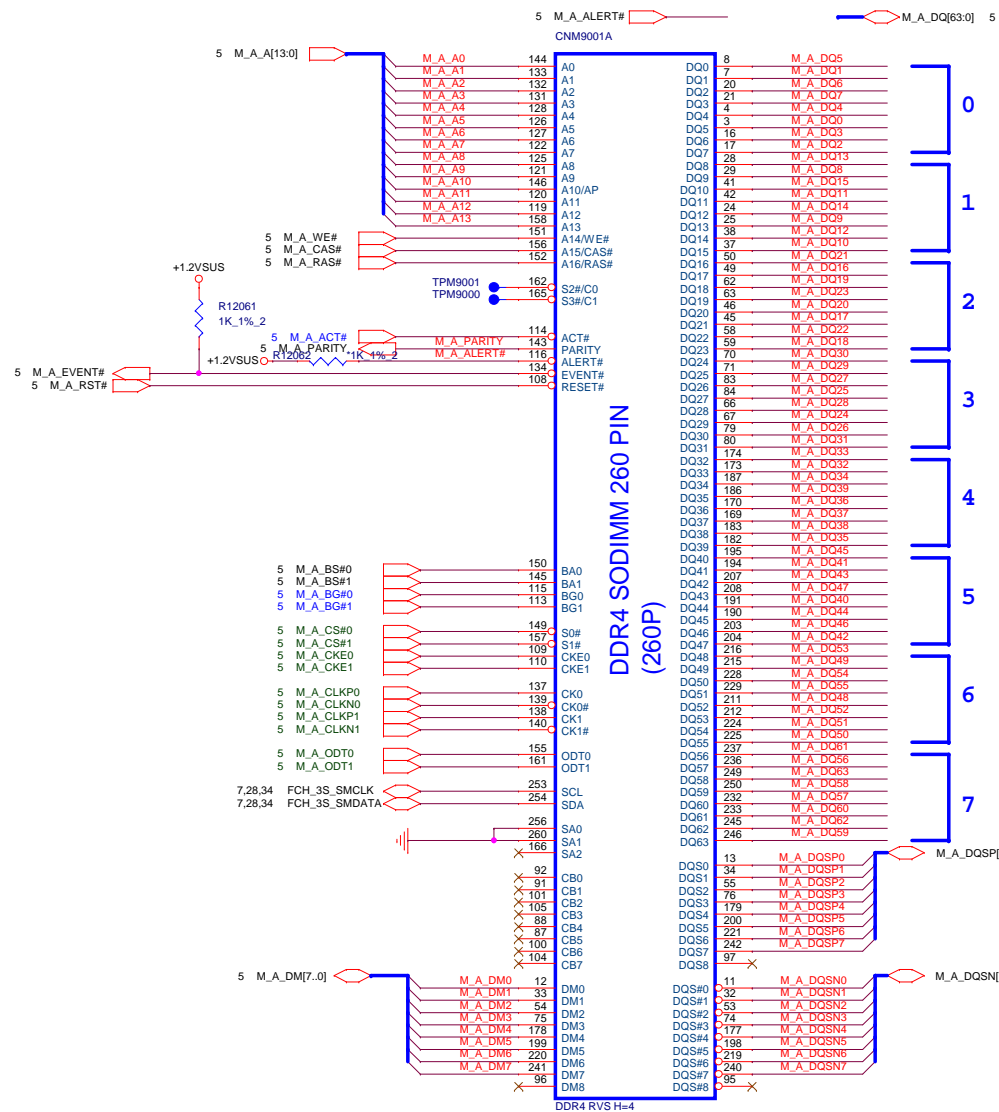


1uF/10uF 4pcs on each side of SODIMM

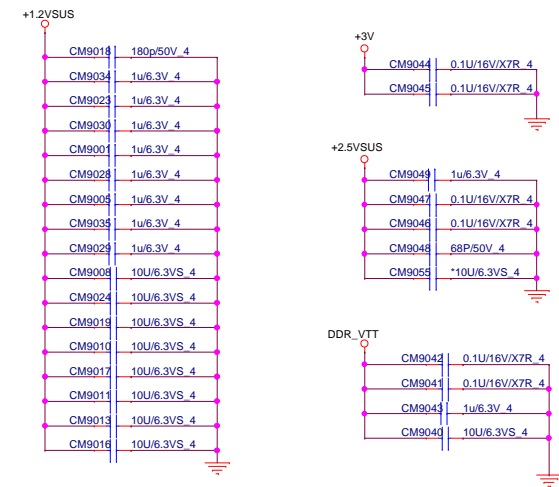


For EMI CAP





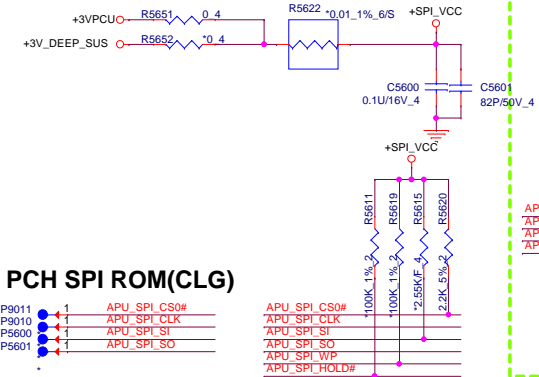
Place these Caps near SODIMM



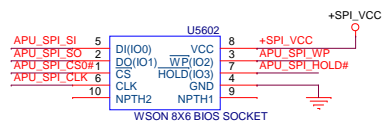


# SPI ROM

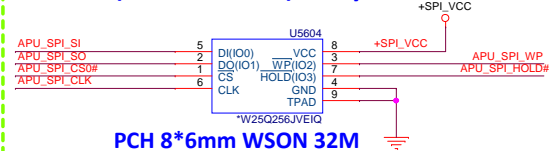
Vender	Size	P/N
MXIC		
Winbond		
Socket		
MXIC		
Winbond		



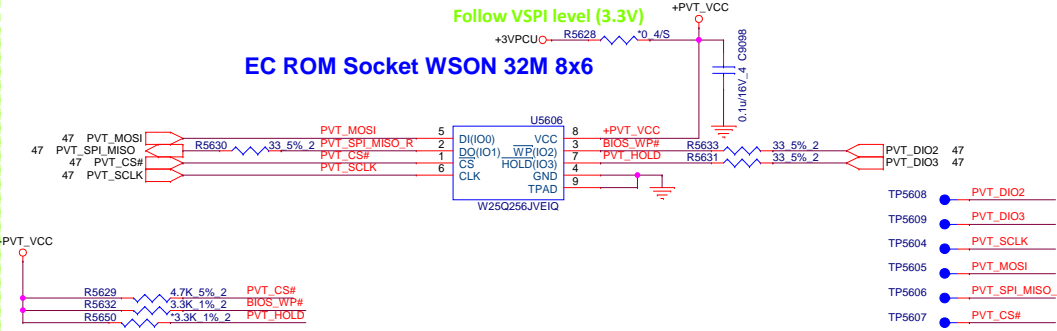
## SPI ROM Socket APU 8\*6mm SPI ROM Socket



## SPI ROM 32M 8x6 IC & 8\*6 Socket (U5602/U5604)co-lay



## EC ROM Socket WSON 32M 8x6

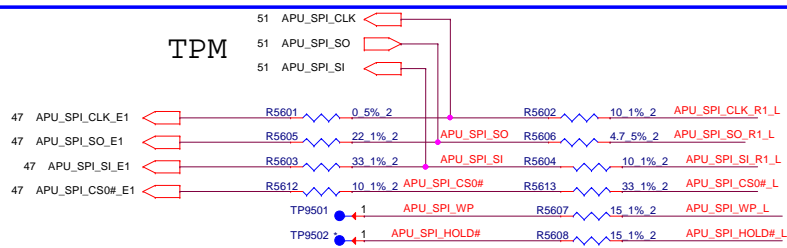


## EC SPI ROM

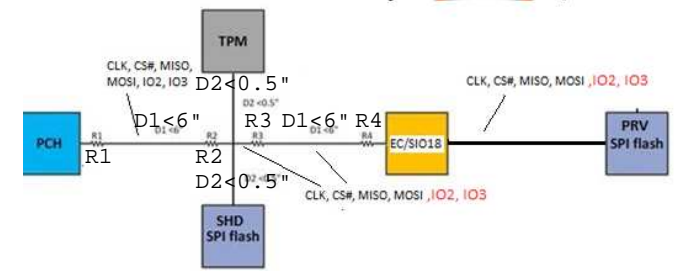
Vender	Size	P/N
		Pilot run stage
		MV stage

## EC

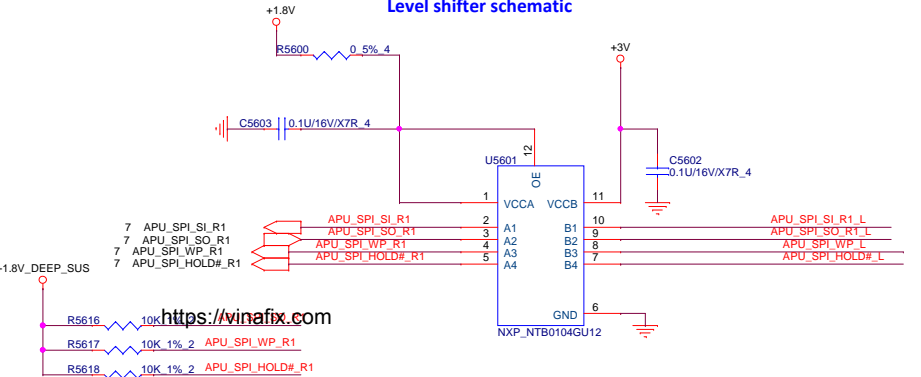
## TPM



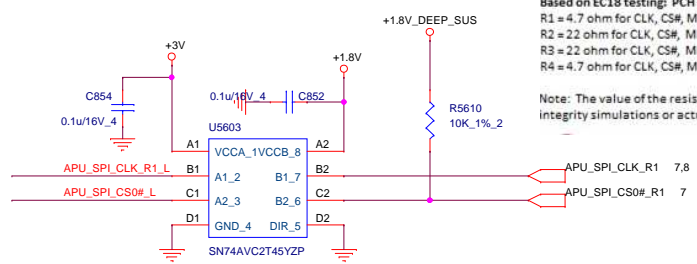
Placing resistor close to cross VIA  
Routing to EC under 6000mil



## Level shifter schematic



Placing resistor close to cross VIA  
Routing to CPU under 6000mil



nuvoton

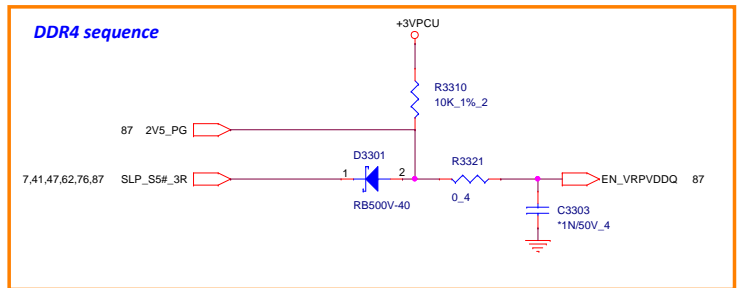
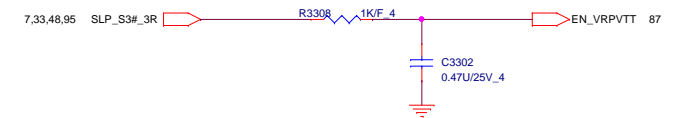
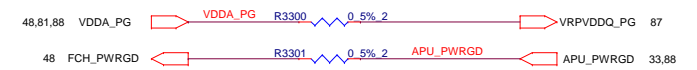
Nuvoton Confidential - Provided under NDA

Based on EC18 testing: PCH to TPM/SPI flash = Quad I/O, SIO18 to SPI Flash = Quad I/O, R1 = 4.7 ohm for CLK, CS#, MISO, MOSI; R1 = 0 ohm for IO2, IO3, R2 = 22 ohm for CLK, CS#, MISO, MOSI; R2 = 15 ohm for IO2, IO3, R3 = 22 ohm for CLK, CS#, MISO, MOSI; R3 = for IO2, IO3 22 ohm, R4 = 4.7 ohm for CLK, CS#, MISO, MOSI; R4 = for IO2, IO3 4.7 ohm

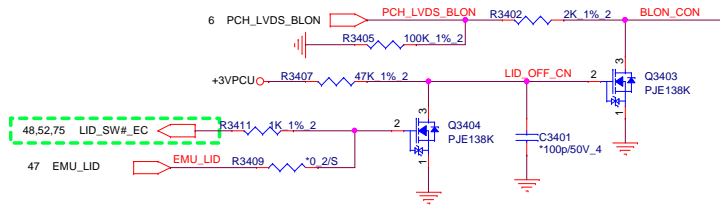
Note: The value of the resistors should be tuned according to the signal integrity simulations or actual PCB measurements.

**PROJECT : 400 G7 AMD**  
**Quanta Computer Inc.**

Size	Document Number	Flash(KBC+PCH)	Rev 1A
Date: Monday, December 07, 2020	Sheet 32	of 68	

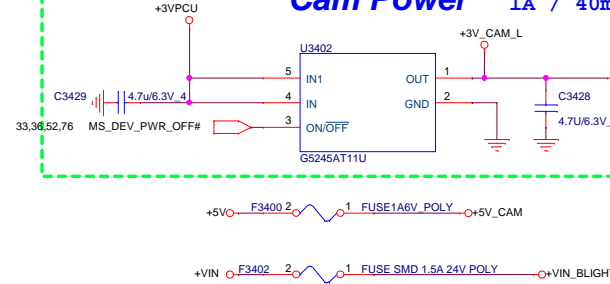


# LID Switch



## For MS

## Cam Power 1A / 40mils

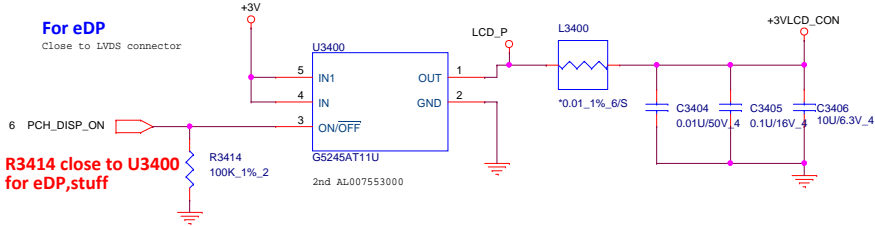


34

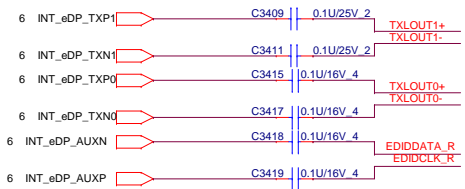
GS12401-1011-9H  
51693-0400-v01-40p-I  
DFFC40FR103

## For eDP

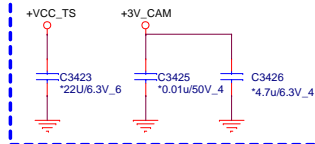
Close to LVDS connector



R3414 close to U3400  
for eDP,stuff



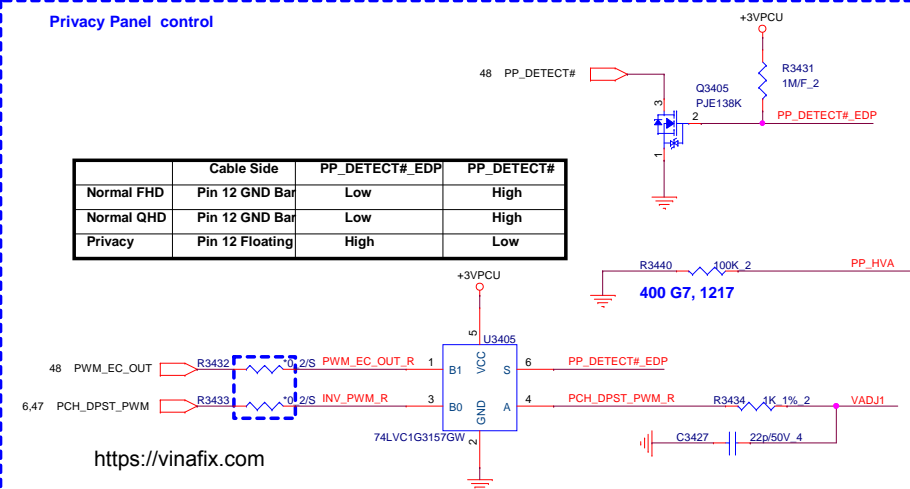
## EMI CAP



Vinafix.com

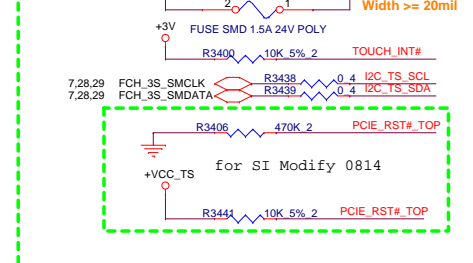
## Privacy Panel control

	Cable Side	PP_DETECT#_EDP	PP_DETECT#
Normal FHD	Pin 12 GND Bar	Low	High
Normal QHD	Pin 12 GND Bar	Low	High
Privacy	Pin 12 Floating	High	Low



https://vinafix.com

## for TS



6,7,8,9,19,20,28,29,32,33,35,36,41,43,47,48,52,54,61,61,95  
20,35,50,54,95  
19,20,33,72,82,86,87,88,89,90,92,93,97

**PROJECT : 400\_600\_G8**  
Quanta Computer Inc.

Size Custom	Document Number 34 - LCD CONN/LID/CAM/D-MIC	Rev 3A
Date: Monday, December 07, 2020	Sheet	34 of 106

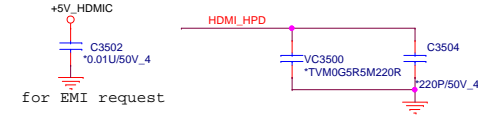
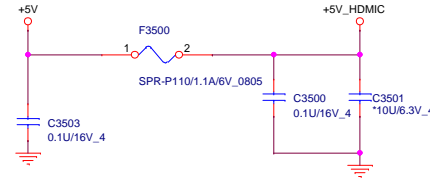
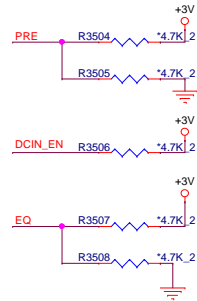
## EMI Solution

TX2_HDMI+	R3500	*150 5% 2	TX2_HDMI-
TX1_HDMI+	R3501	*150 5% 2	TX1_HDMI-
TX0_HDMI+	R3502	*150 5% 2	TX0_HDMI-
TXC_HDMI+	R3503	*150 5% 2	TXC_HDMI-

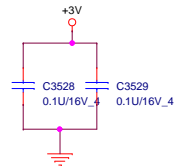
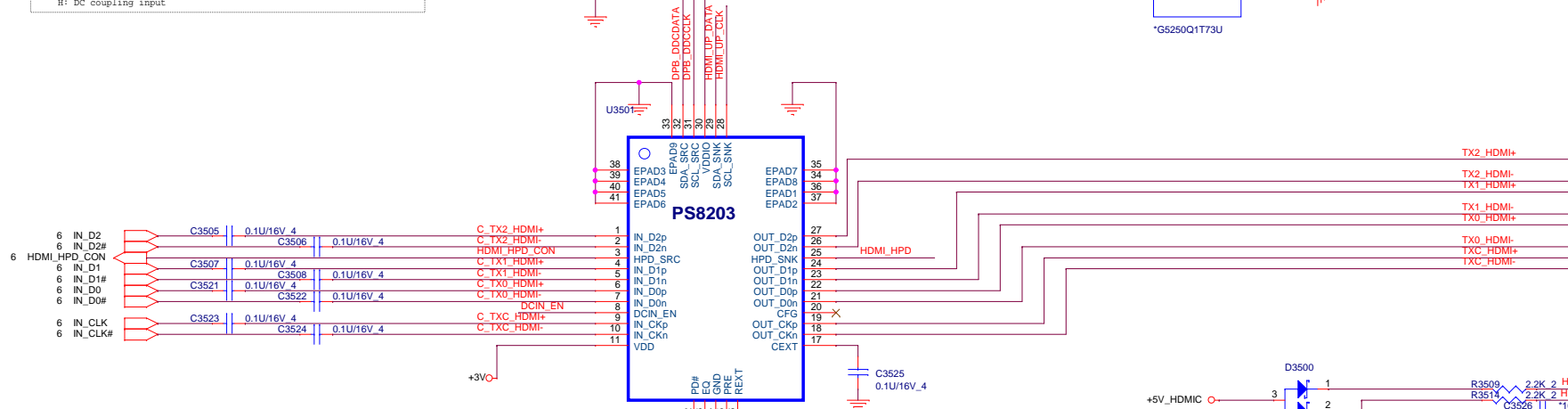
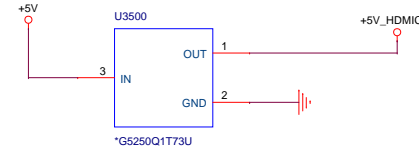
Output pre-emphasis setting; Internal pull down at ~150k $\Omega$ , 3.3V I/O.  
L: no pre-emphasis  
H: 2.5dB pre-emphasis

Receiver equalization setting; Internal pull down at ~150k $\Omega$ , 3.3V I/O.  
L: programmable EQ for channel loss up to 12.4dB @ 3Gbps  
H: programmable EQ for channel loss up to 4.3dB @ 3Gbps  
M: programmable EQ for channel loss up to 8.6dB @ 3Gbps

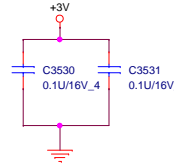
DC coupling enable; Internal pull down at ~150k $\Omega$ , 3.3V I/O.  
L: default, AC coupling input  
H: DC coupling input



for EMI request

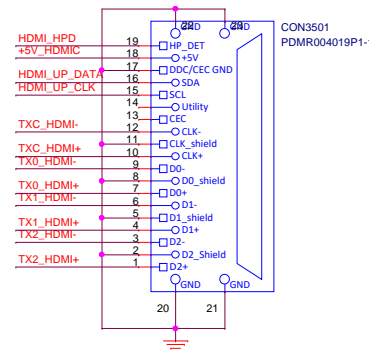
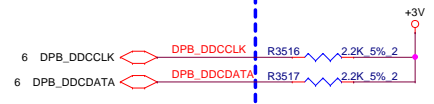


VDD for PS8203:  
Power supply at 3.3V

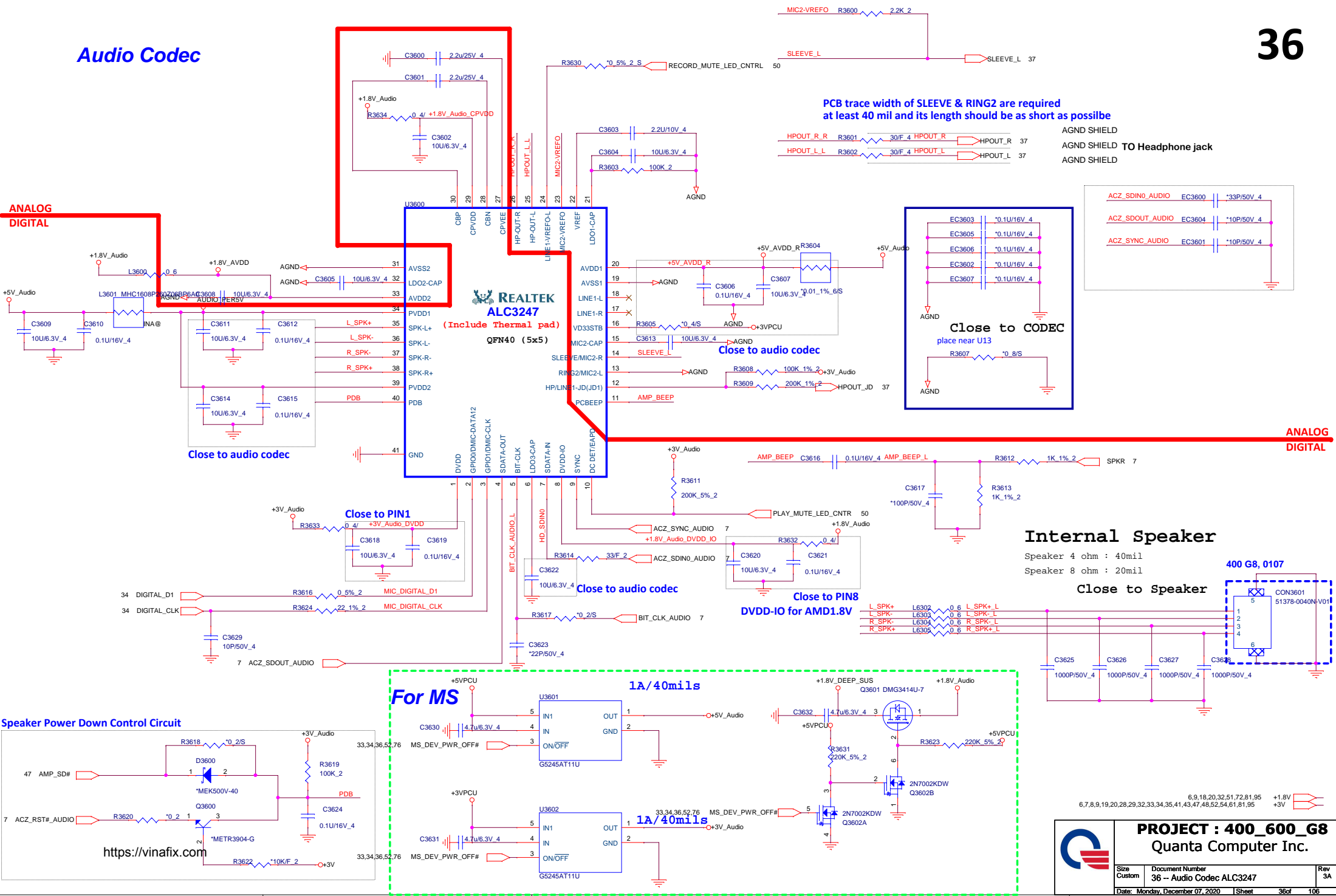


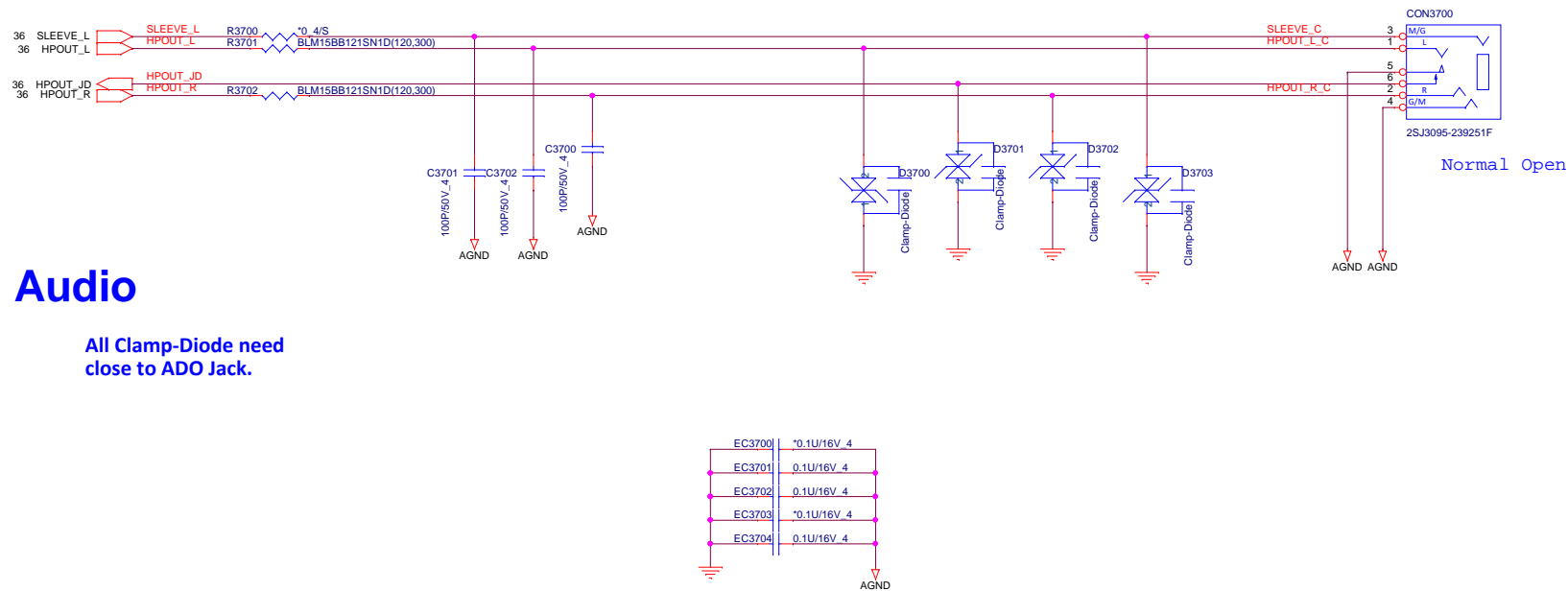
VDDIO:  
Supply voltage for DDC passive gate and used to set HPD\_SRC output level  
Its range can be 1.2V~3.6V

## HDMI SMBus Isolation



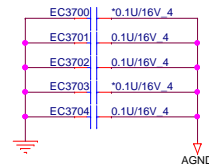
## Audio Codec


ANALOG  
DIGITAL



## Audio

All Clamp-Diode need close to ADO Jack.



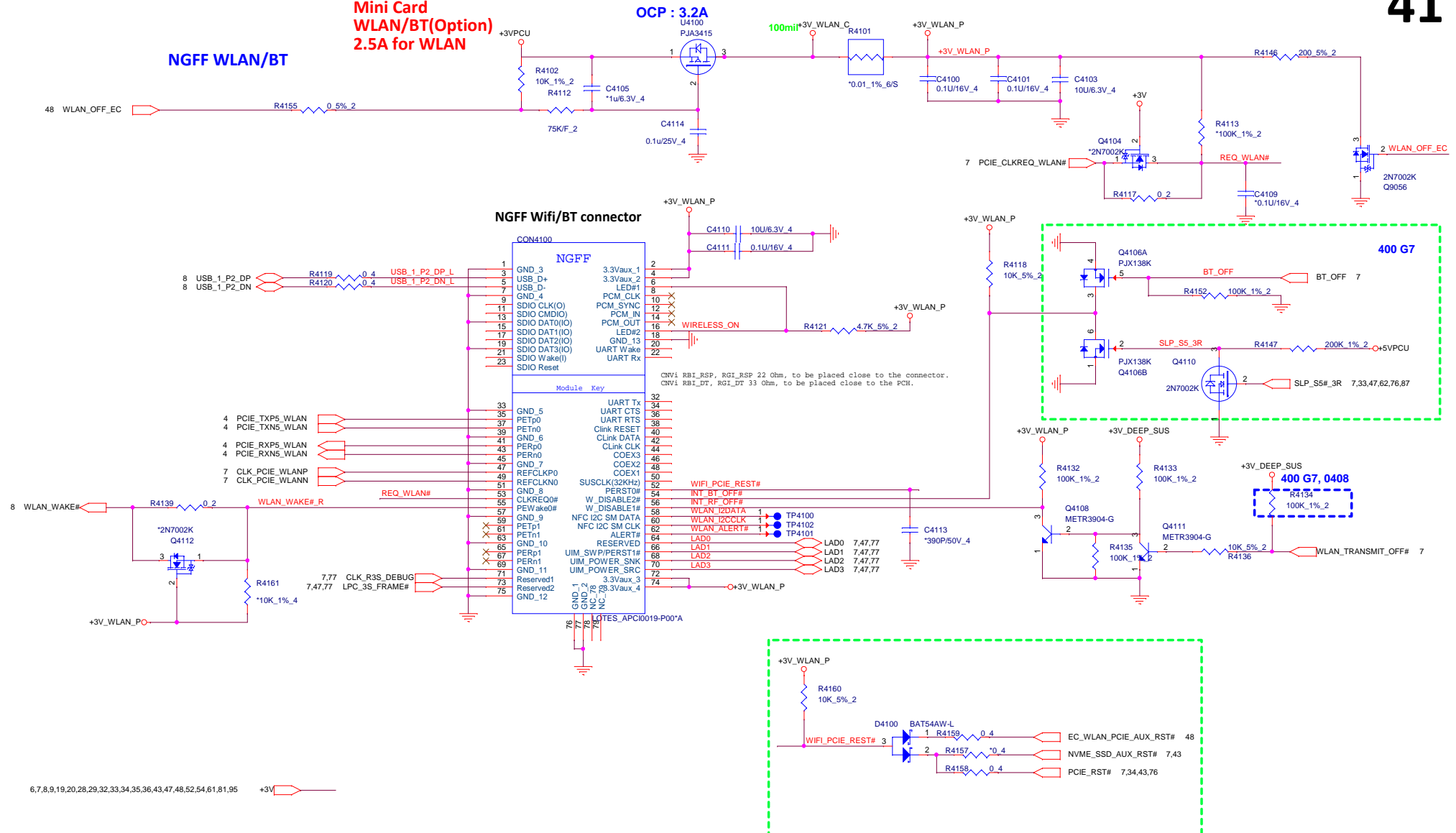


**PROJECT : 400\_600\_G8**  
**Quanta Computer Inc.**

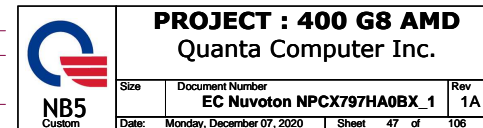
Size Custom	Document Number <b>40 -- LAN RTL8111HSH-CG/RJ45</b>	Rev 3A
Date: Monday, December 07, 2020		Sheet 40 of 106



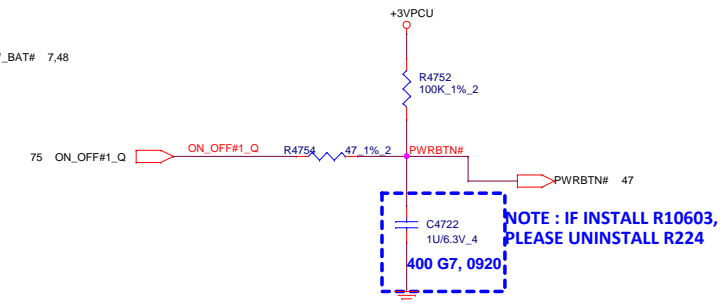
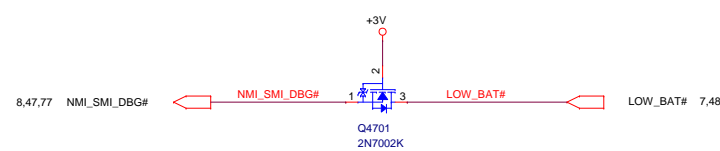
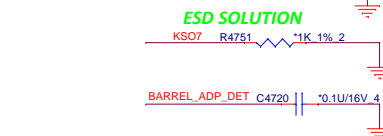
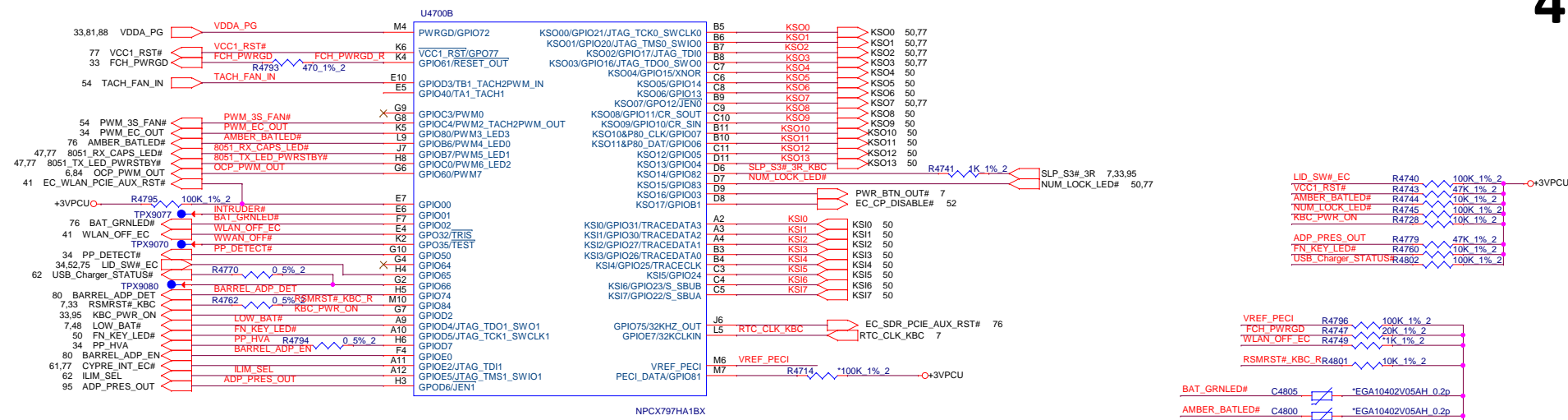
**Mini Card  
WLAN/BT(Optional)  
2.5A for WLAN**



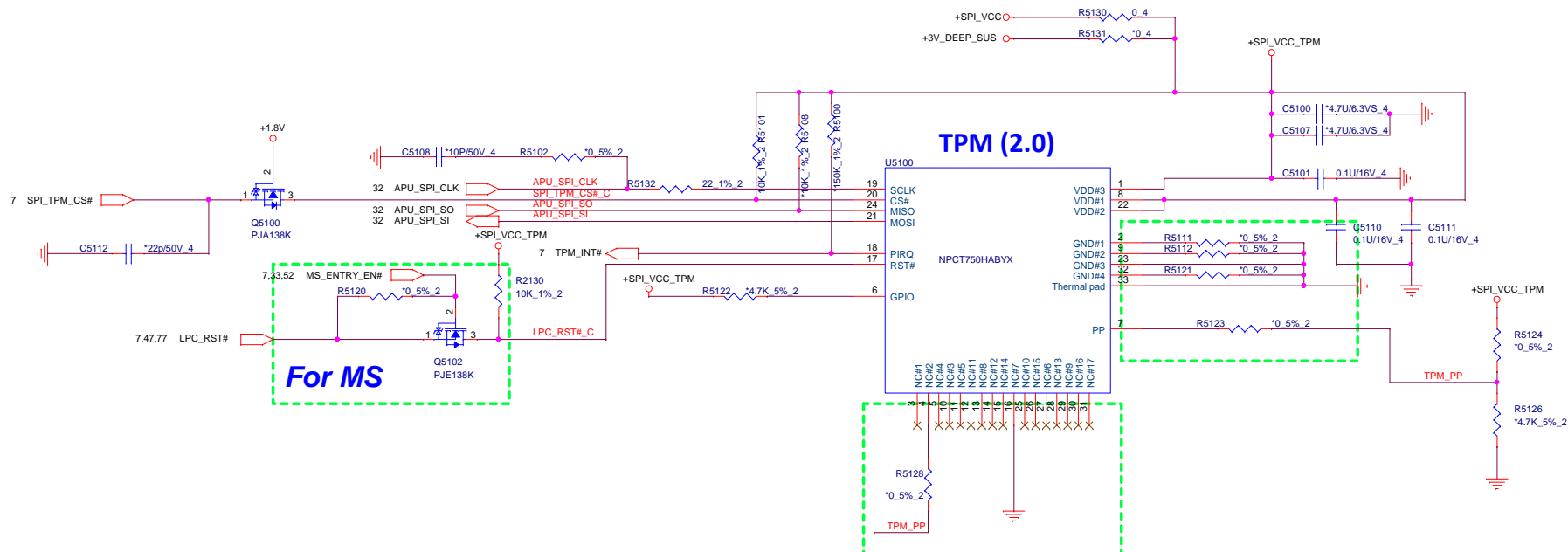


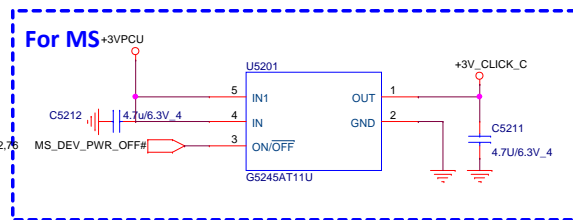
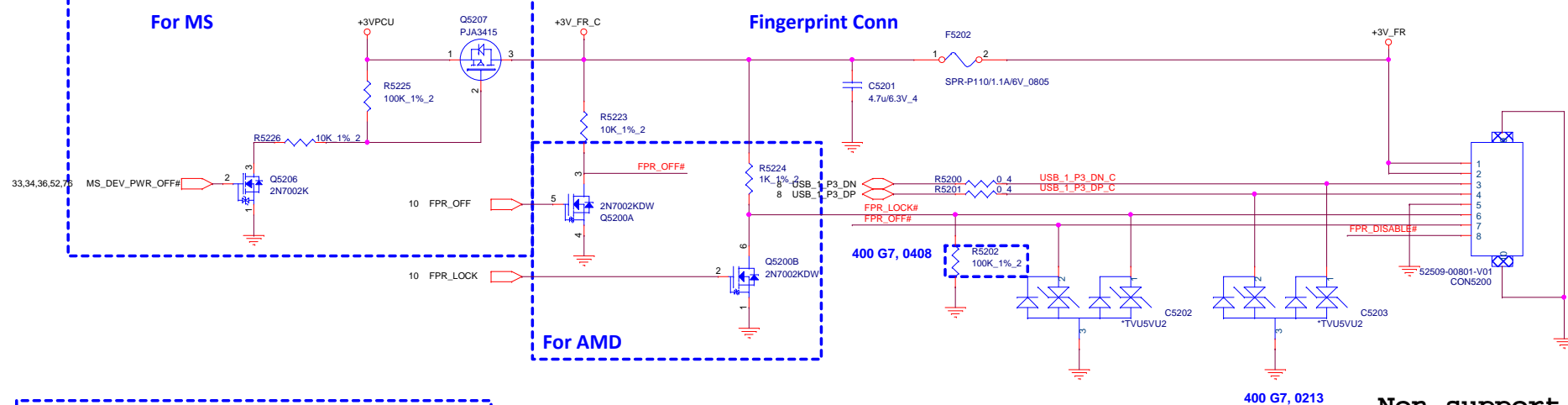


All the PWM outputs can directly drive the cathode of a LED connected to 3.3V power

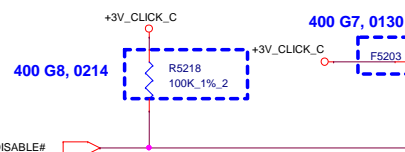
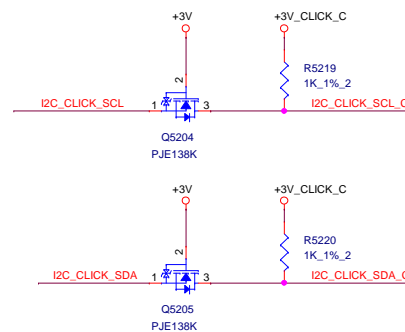
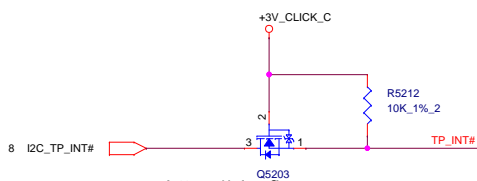
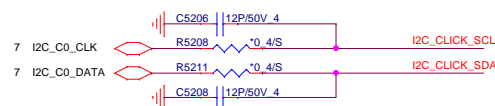
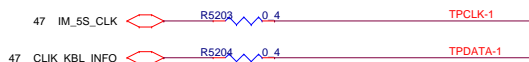
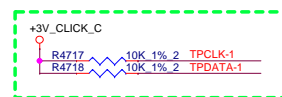




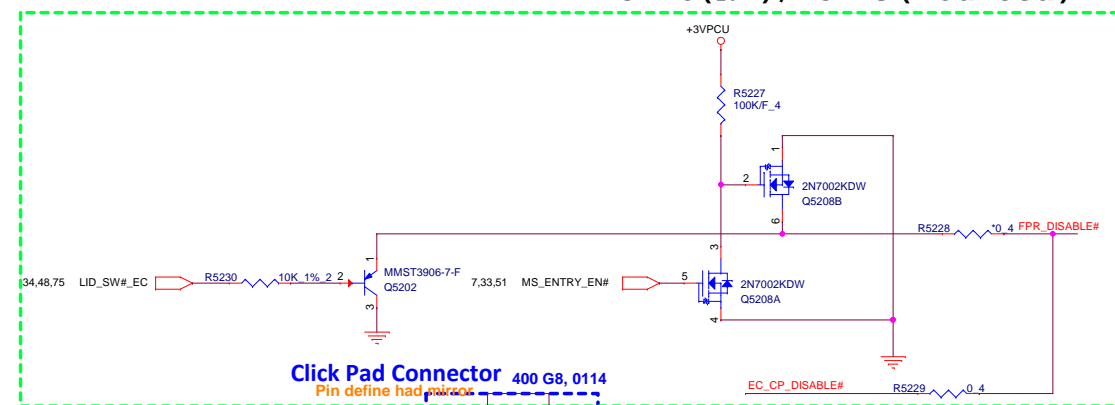




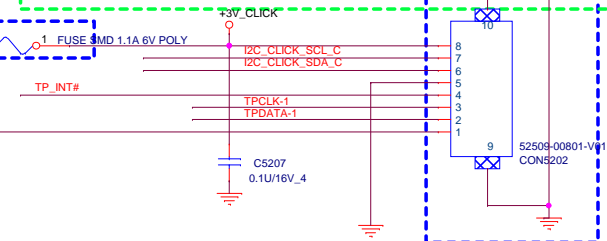
**Non support Wake UP on FPR:  
R5228(mounted )/R5229(NI)  
Support Wake UP on FPR:  
R5228(NI)/R5229(mounted)**



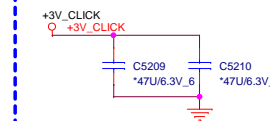
**CLICK PAD**  
Address: 0x20(7 bit)



**Click Pad Connector 400 G8, 0114**  
Pin define had mirror



**EMI CAP**



Pin	Connector1(TP)
1	VDD
2	I2C-CLK
3	I2C-Data
4	GND
5	I2C_INT
6	Not used (reserved for PS2-CLK)
7	KB_BL_EN# (reserved for PS2-Data)
8	TP-Disable#

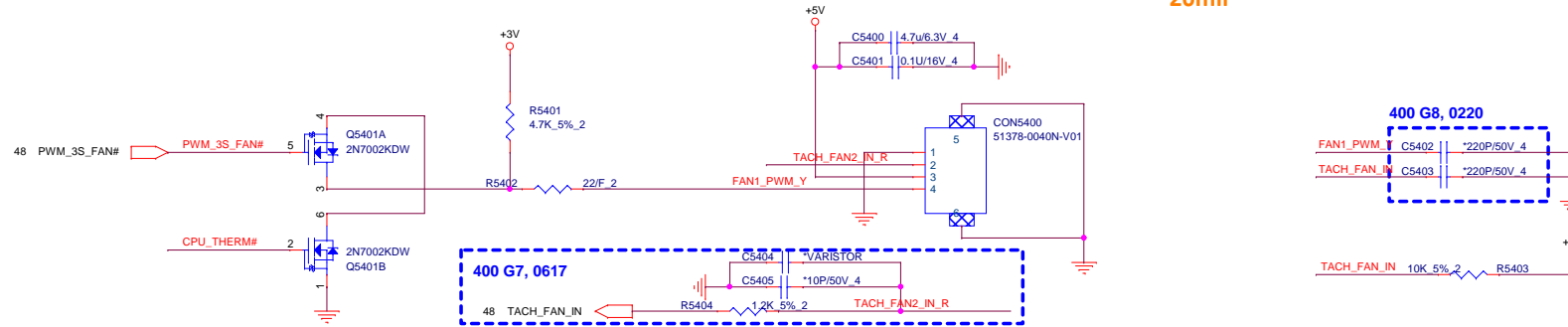
<https://vinafix.com>

**PROJECT : 400\_600\_G8**  
Quanta Computer Inc.

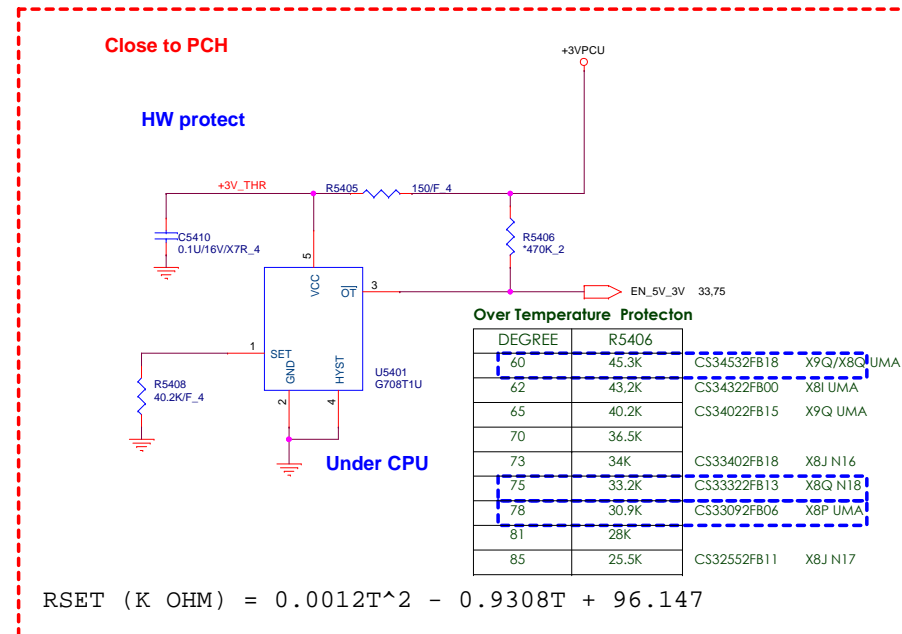
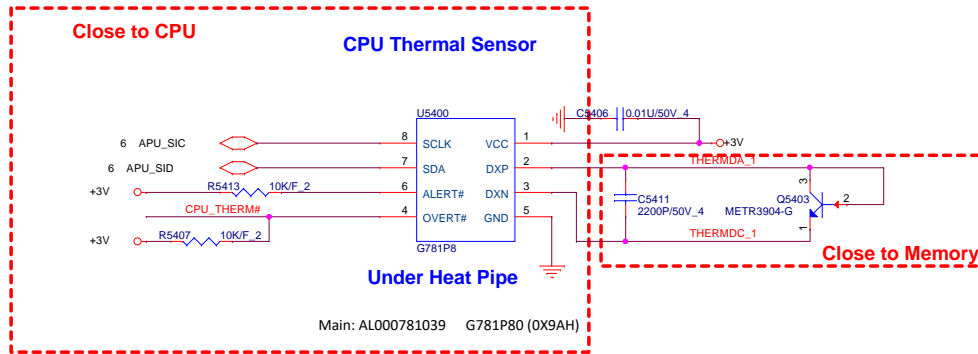
Size Custom	Document Number 52 -- FPR / Click PAD	Rev 3A
Date: Monday, December 07, 2020	Sheet 52 of 106	





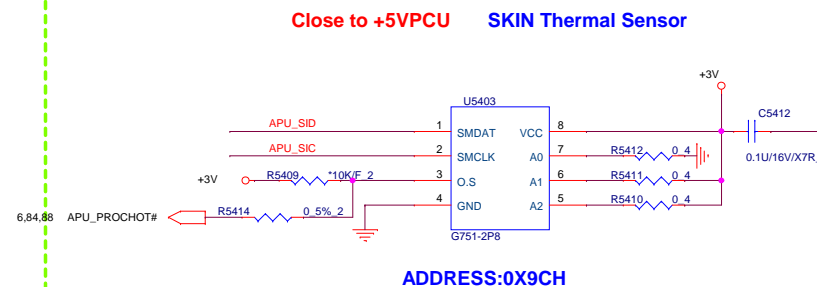


## Thermal sensor



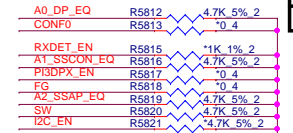
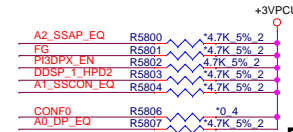
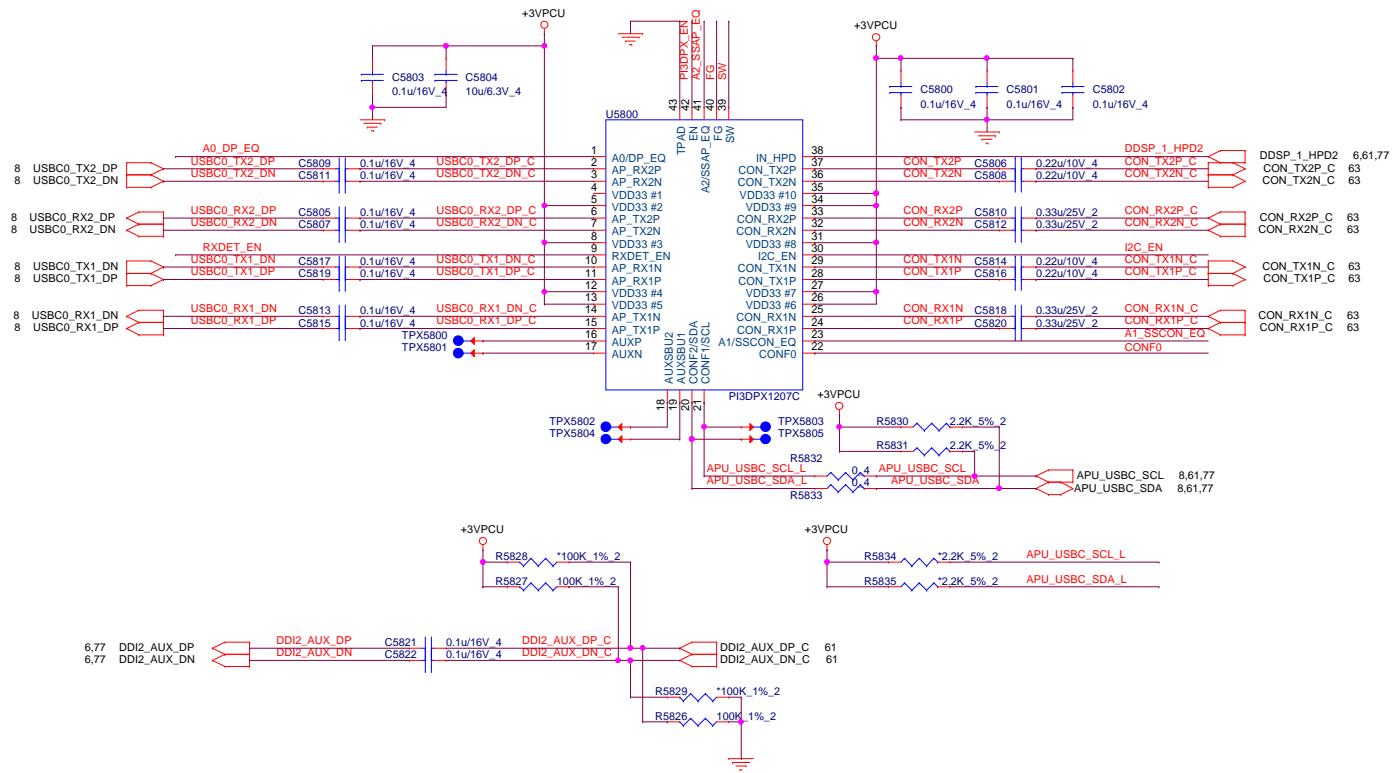
Vinafix.com

For AMD

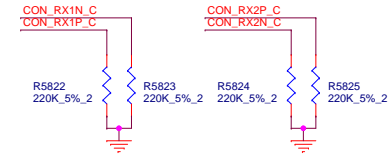


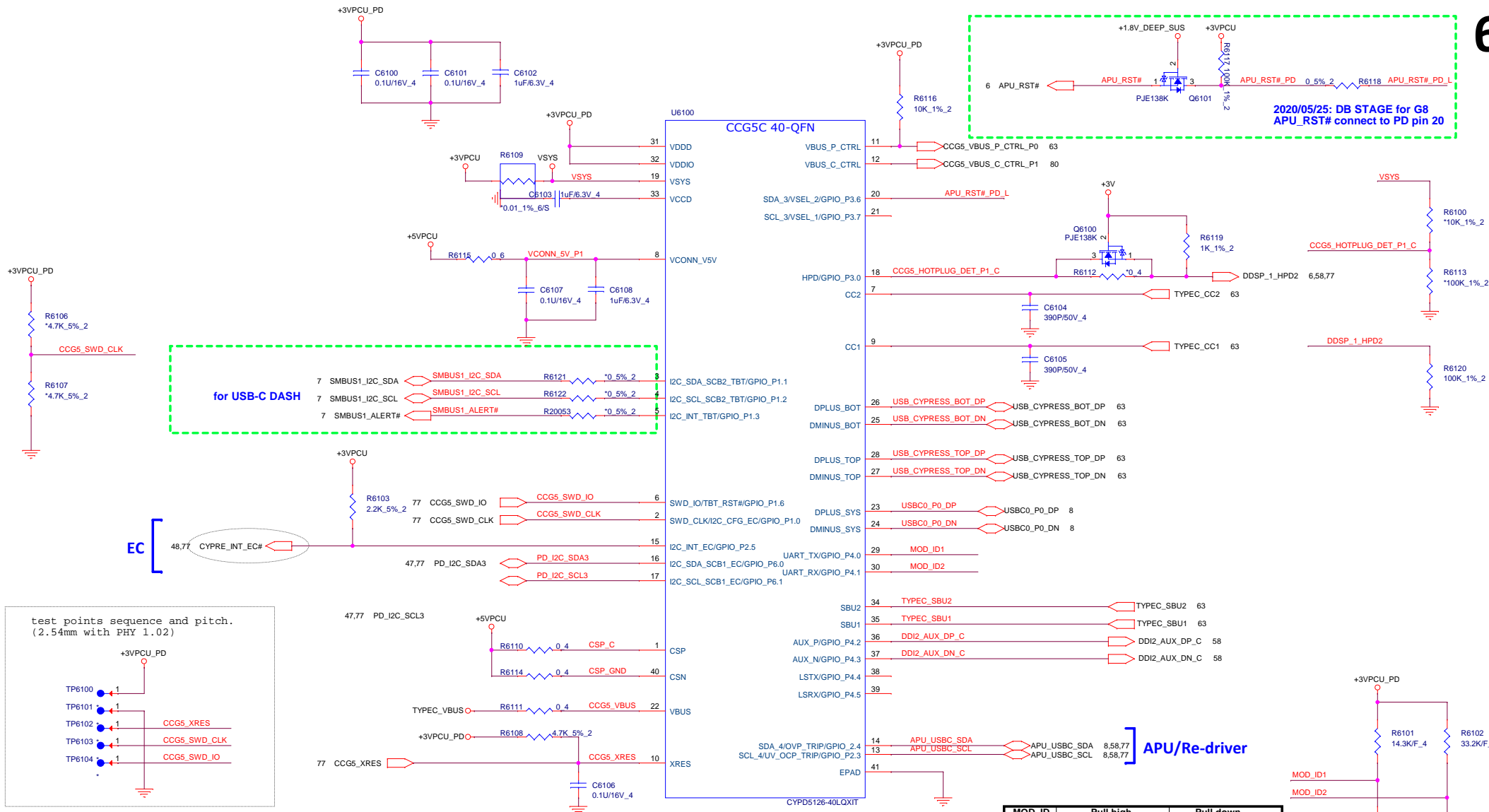
6,7,8,9,19,20,28,29,32,33,34,35,36,41,43,47,48,52,61,81,95

+3V



	PULL UP	PULL DOWN
A0_DP_EQ	X	4.7K
A1_SSCON_EQ	X	4.7K
A2_SSAP_EQ	X	4.7K





	Platform ID	CCG5 Dual Port	CCG5/CCG5C Single Port	
	MOD_ID1	MOD_ID2	Description (Dual port)	Description (Single Port)
Notebooks	L8	L7	Reserved	DRP+USB on 1-port with No MUX
	L7	L7	DRP+DP+ AR TBT on 2-ports	DRP+DP on 1-port with ANX MUX
	L6	L7	DRP+DP on 2-ports	DRP+DP+ TR TBT on 1-port
	L5	L7	DRP+DP on 2-ports with ANX MUX	DRP+DP+ AR TBT on 1-port (700, 800 Series)
	L4	L7	Malta	DRP+DP on 1-port with Parade MUX
	L3	L7	DRP+DP+ TR TBT on 2-ports	DRP+DP on 1-port (600/700 Series) - AMD SKU1
	L2	L7	Reserved	DRP+DP on 1-port (600/700 Series) - AMD SKU2
	L1	L7	Reserved	DRP+DP on 1-port (600/700 Series) - AMD SKU3
	L0	L7	Reserved	DRP+DP on 1-port with Parade MUX - 2019 S400 G6
	L7	L6	Reserved	DRP+DP on 1-port (400 Series) - AMD

MOD_ID	Pull high	Pull down
L0	None	1K
L1	7.1K	1K
L2	5.9K	2.2K
L5	3.09K	5.1K
L6	33.2K	100K
L7	14.3K	100K



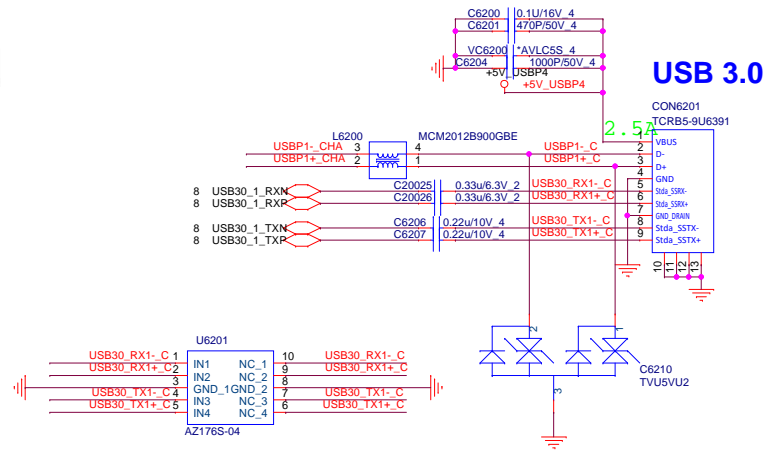
**PROJECT : 400 G7 AMD**  
**Quanta Computer Inc.**

Size	Document Number	Cypress CCG5C	Rev 1A
Date:	Monday, December 07, 2020	Sheet 61 of 106	

### USB Charging Port

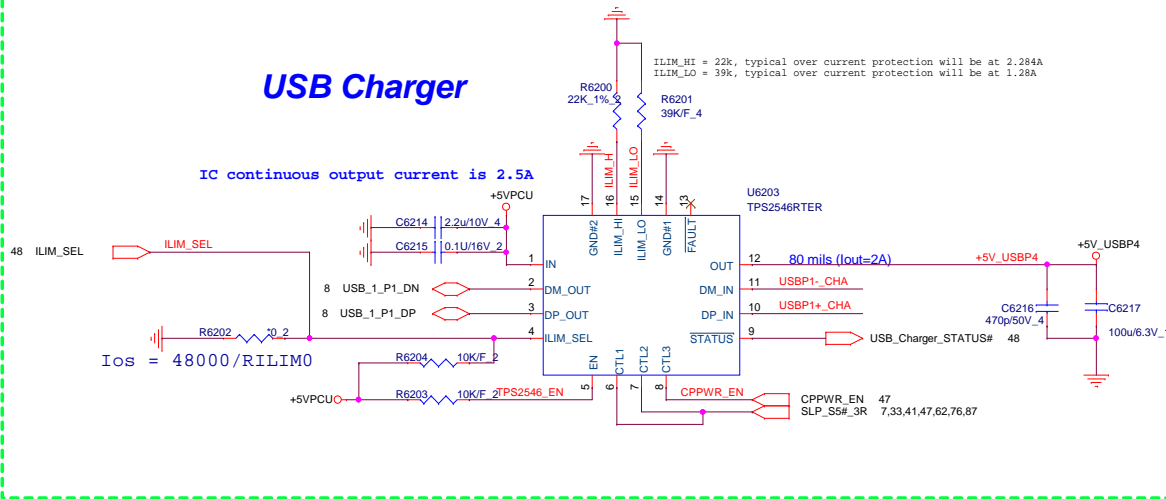


**USB 2.0/3.0 Combo**  
**Right for Charge**



## USB Charger

IC continuous output current is 2.5A

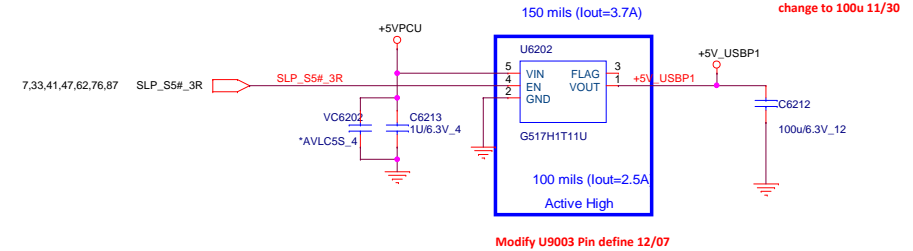
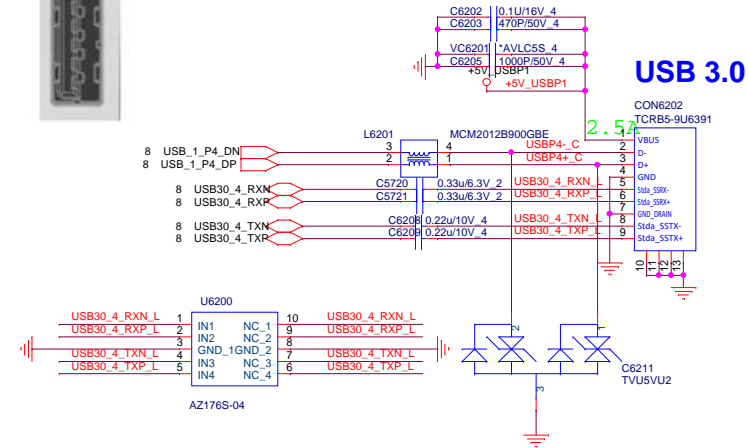


<https://vinafix.com>

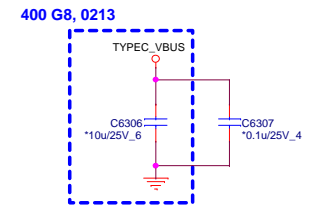
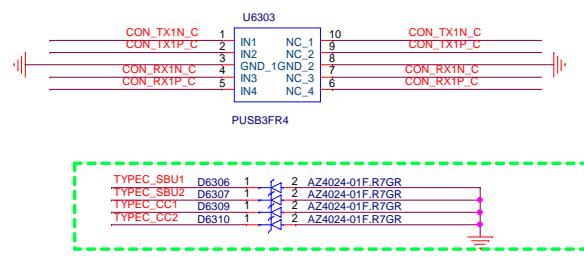
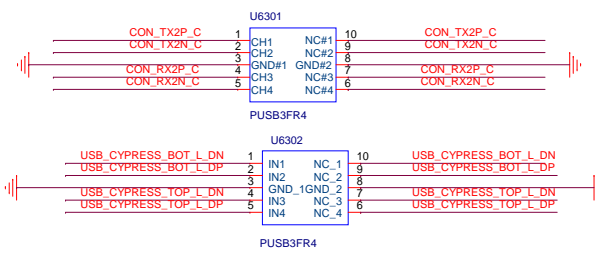
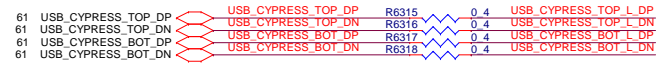
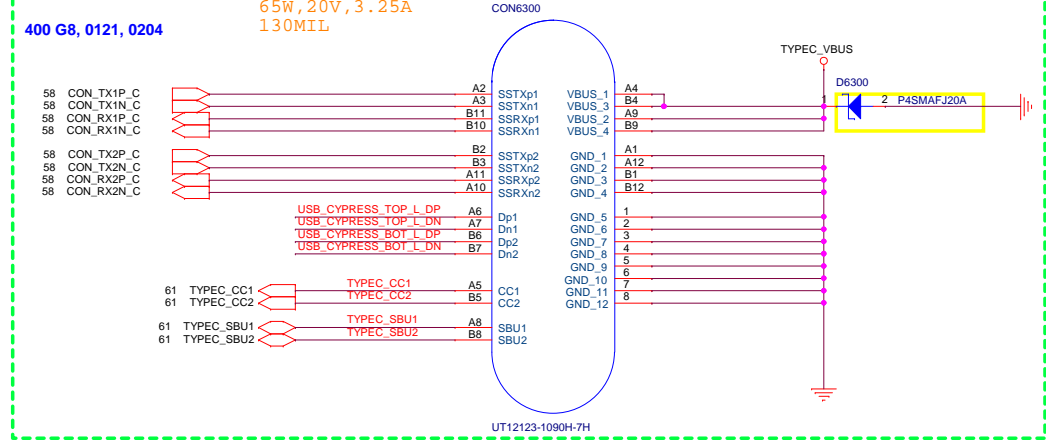
USB Stander Port



### **USB 2.0/3.0 Combo**



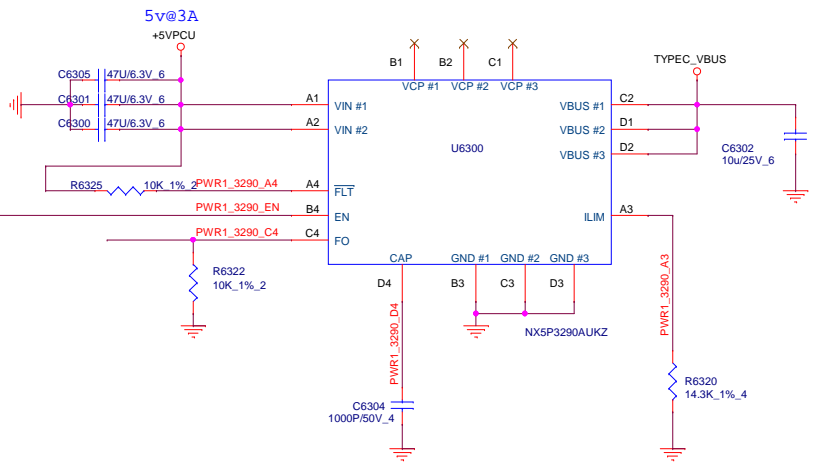
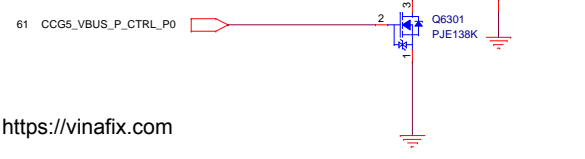
# USB Type-C Port A



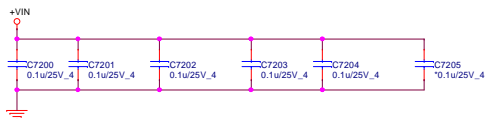
CCG5C\_VBUS\_P\_CTRL\_P1= 0 (Provider Path ON)

CCG5C\_VBUS\_P\_CTRL\_P1= 1 (Provider Path OFF)

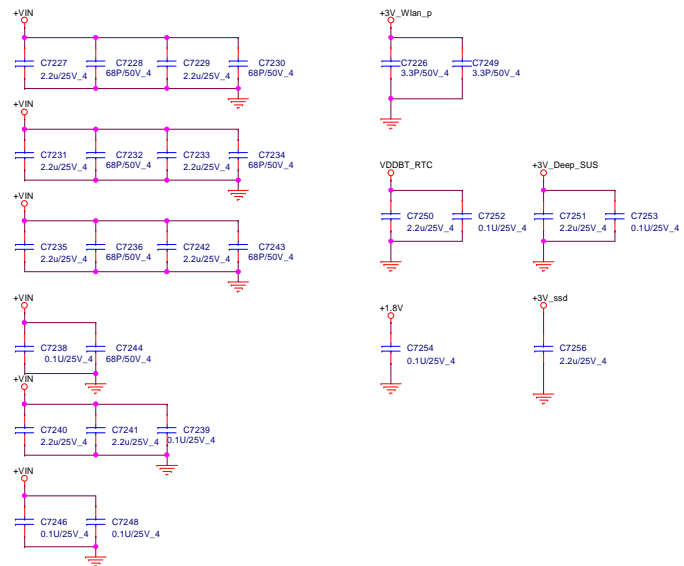
ACTIVE LOW



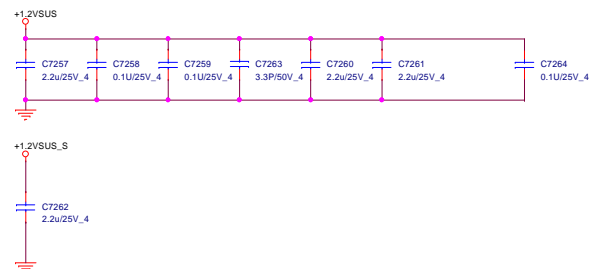
<https://vinafix.com>



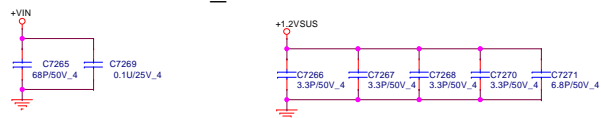
RF New Add CAP\_0526



RF New Add CAP\_0620



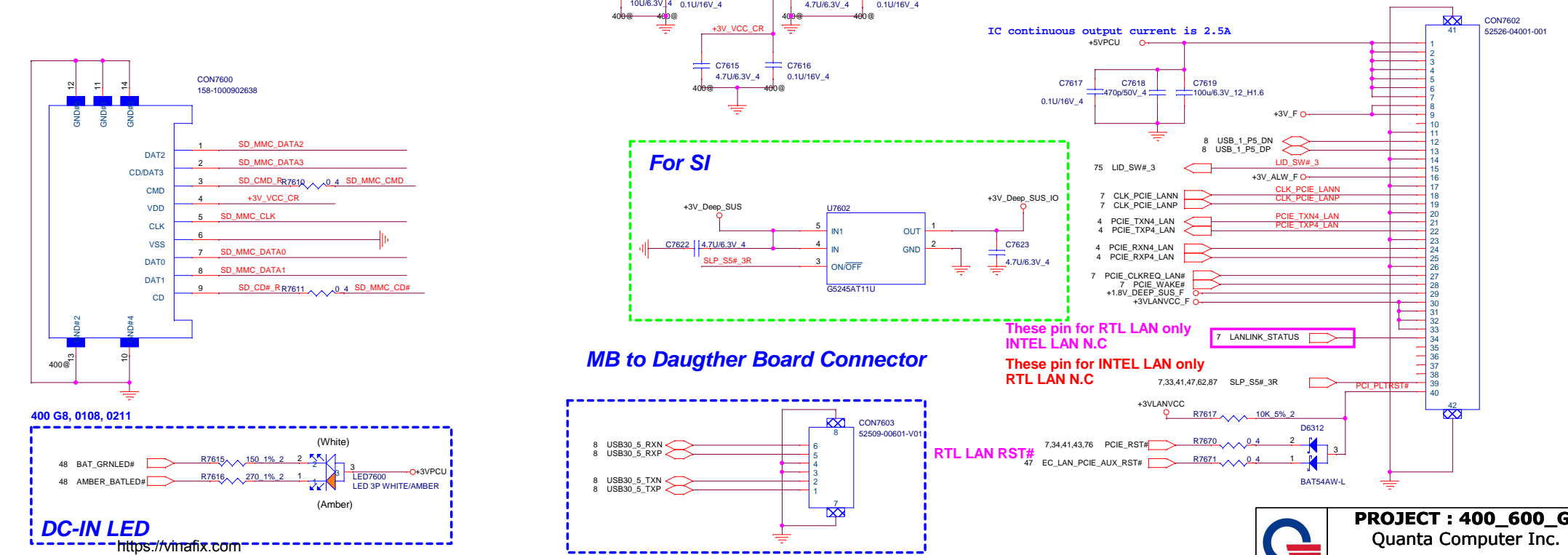
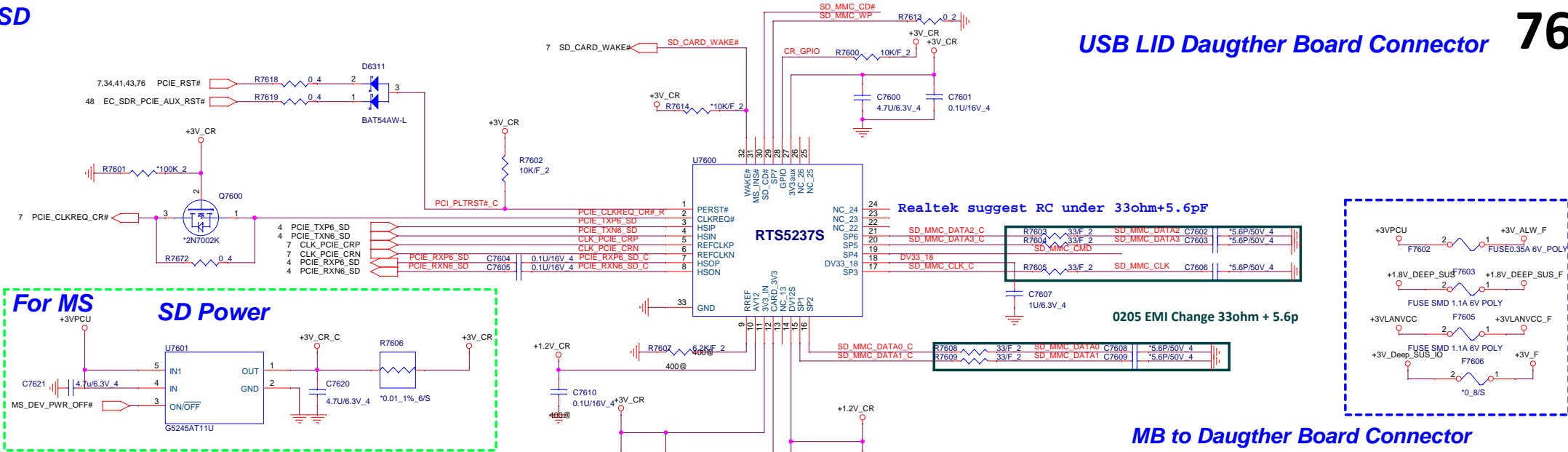
RF New Add CAP\_0817 for SI



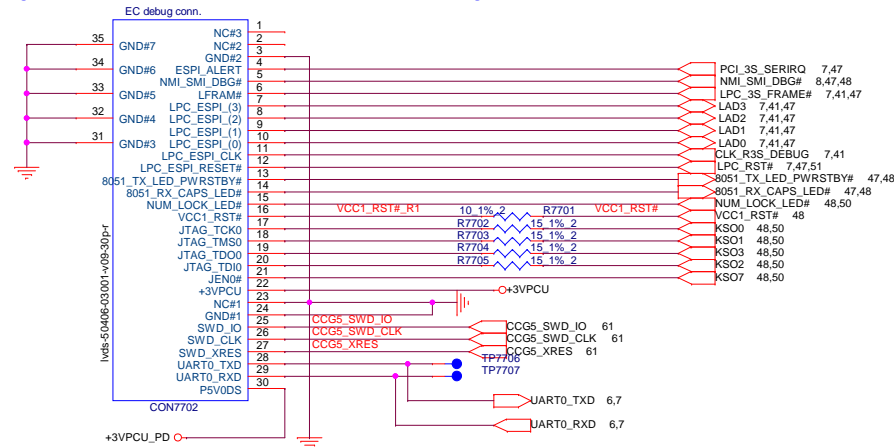


[illegible]

**SD**



## EC debug conn. (From Workstation Venus)

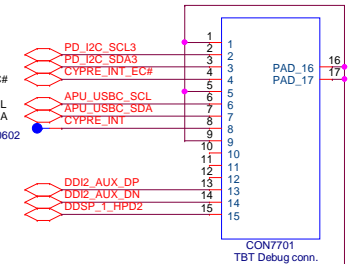


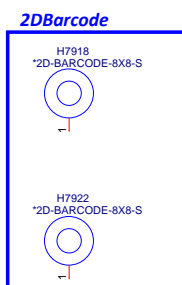
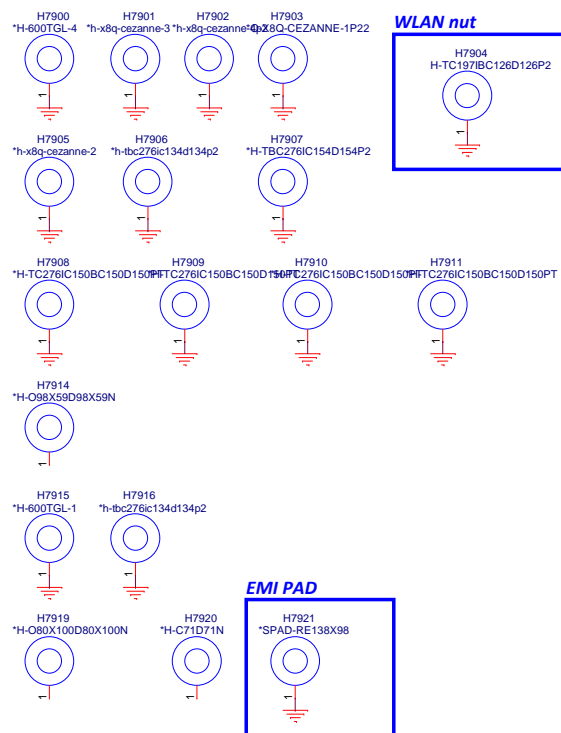
## TYPE-C Debug connector

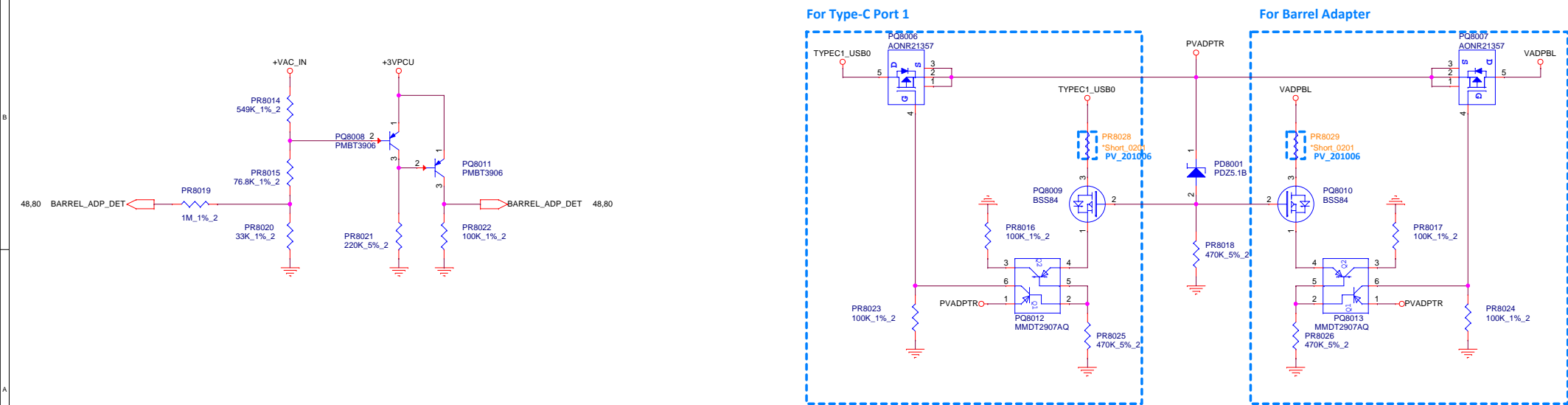
EC  
APU

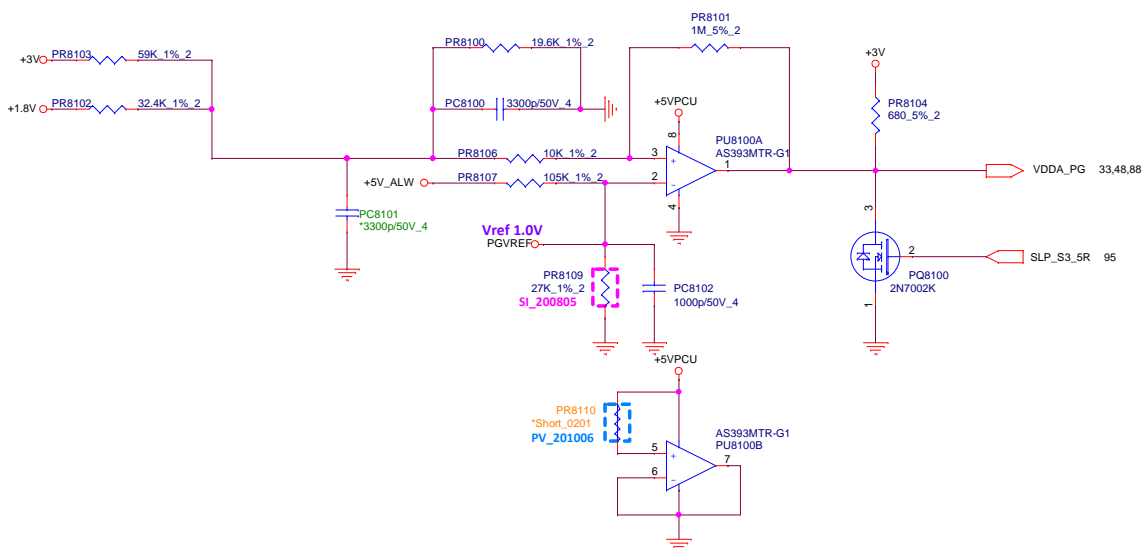
47,61 PD\_I2C\_SCL3  
47,61 PD\_I2C\_SDA3  
48,61 CYPRE\_INT\_EC#  
8,58,61 APU\_USBC\_SCL  
8,58,61 APU\_USBC\_SDA  
TP10602

## TBT Debug conn.










## 82



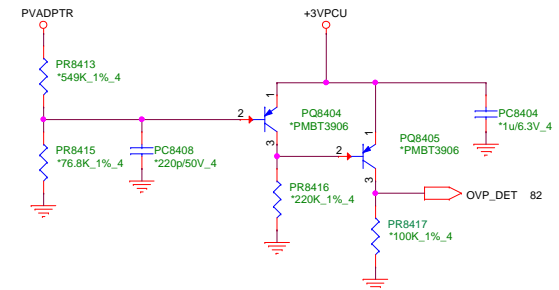
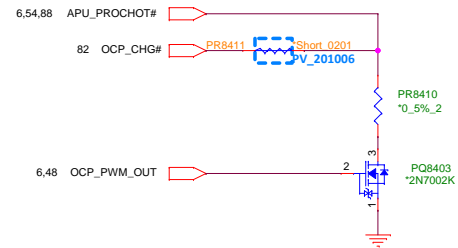
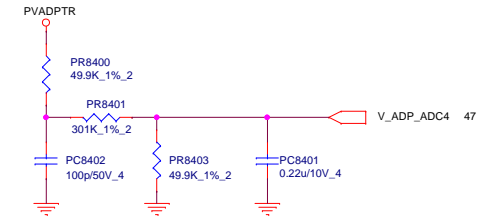
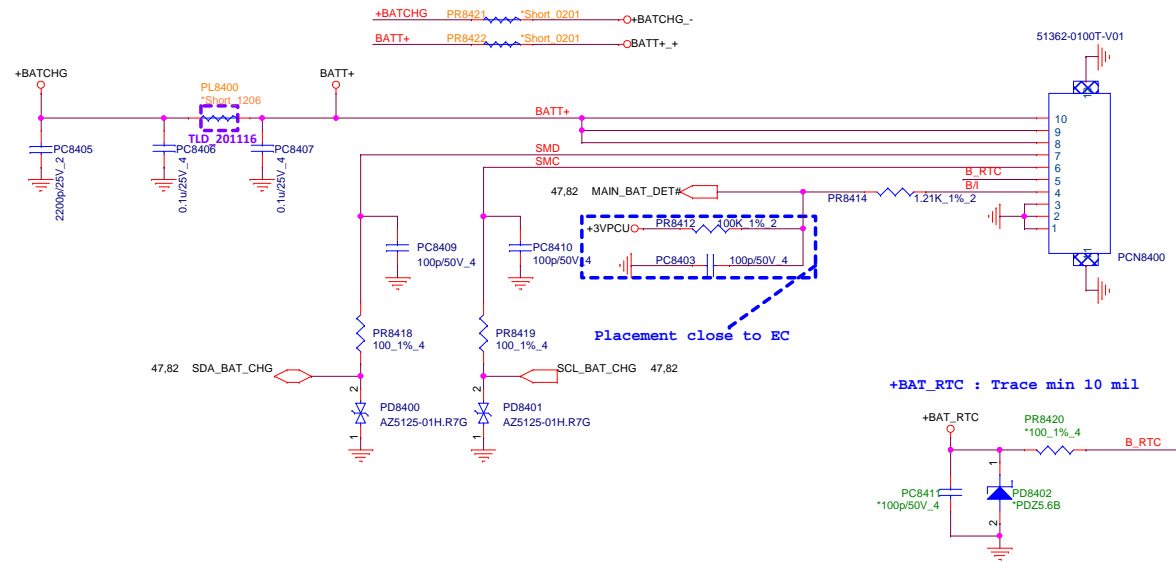
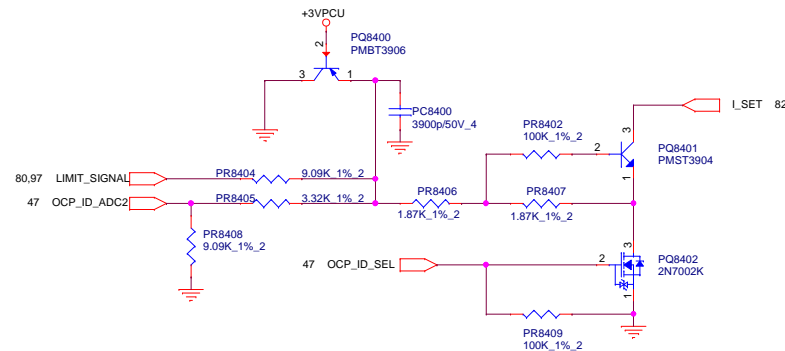



**PROJECT : 400\_600\_G8**  
Quanta Computer Inc.

Size Custom	Document Number <b>83 -- Charger (ISL9538HRTZ-T)</b>	Rev 1A
Date: Monday, December 07, 2020   Sheet 83 of 106		



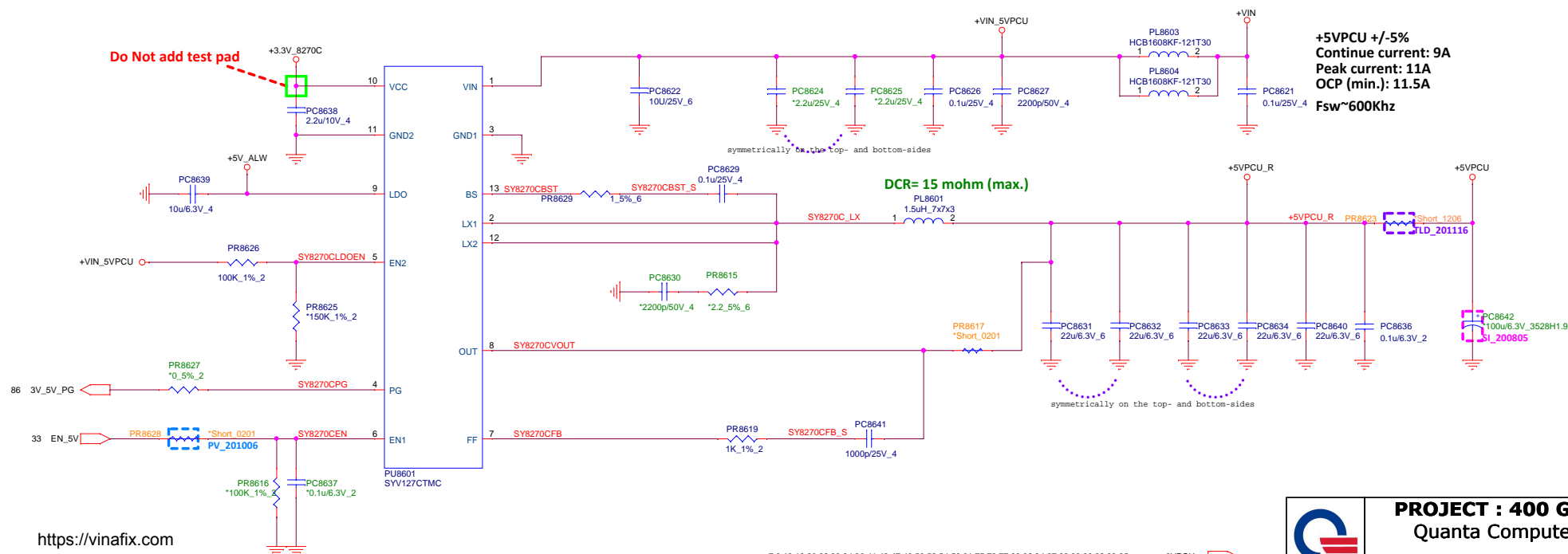
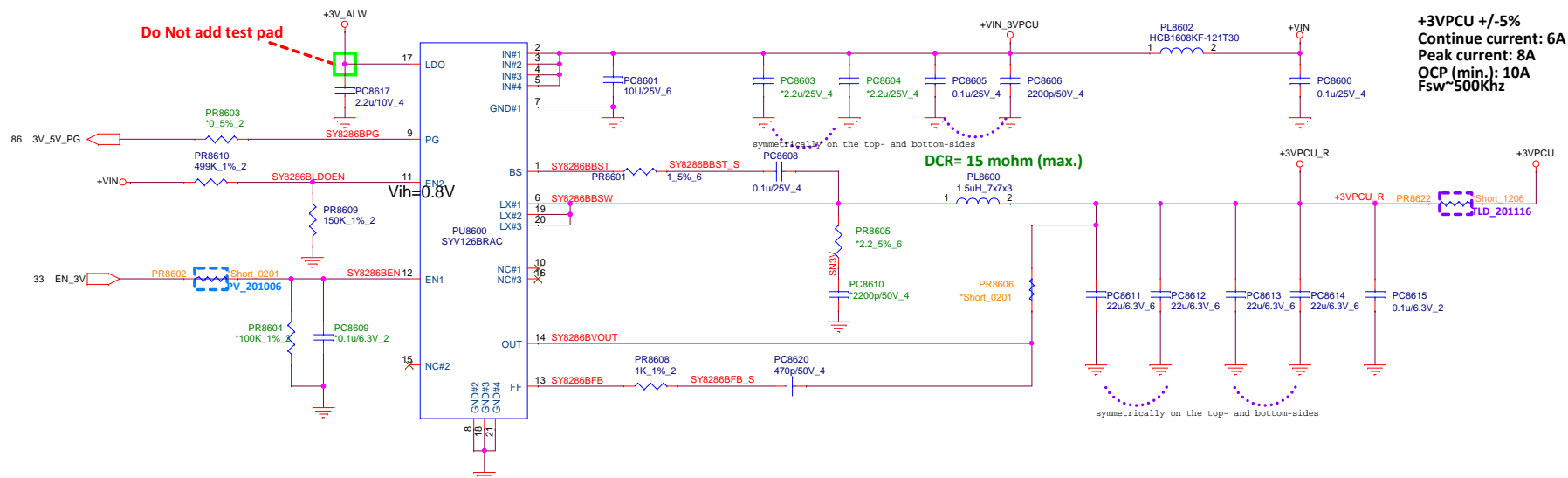
### Barrel Adapter OCP

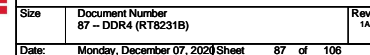




**PROJECT : 400\_600\_G8**  
Quanta Computer Inc.

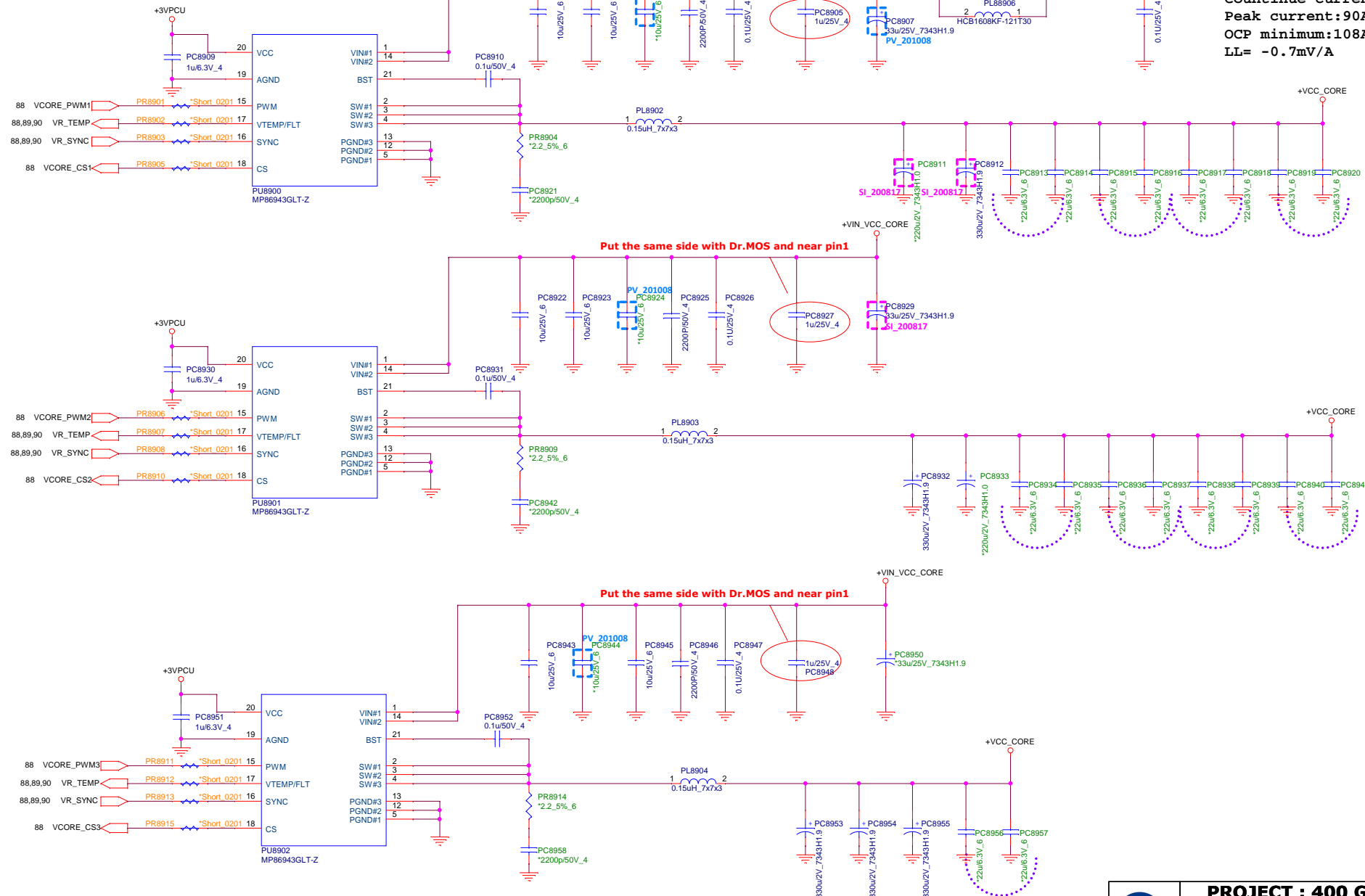
Size Custom	Document Number 85 -- Charger II	Rev 1A
Date: Monday, December 07, 2020   Sheet 85 of 106		

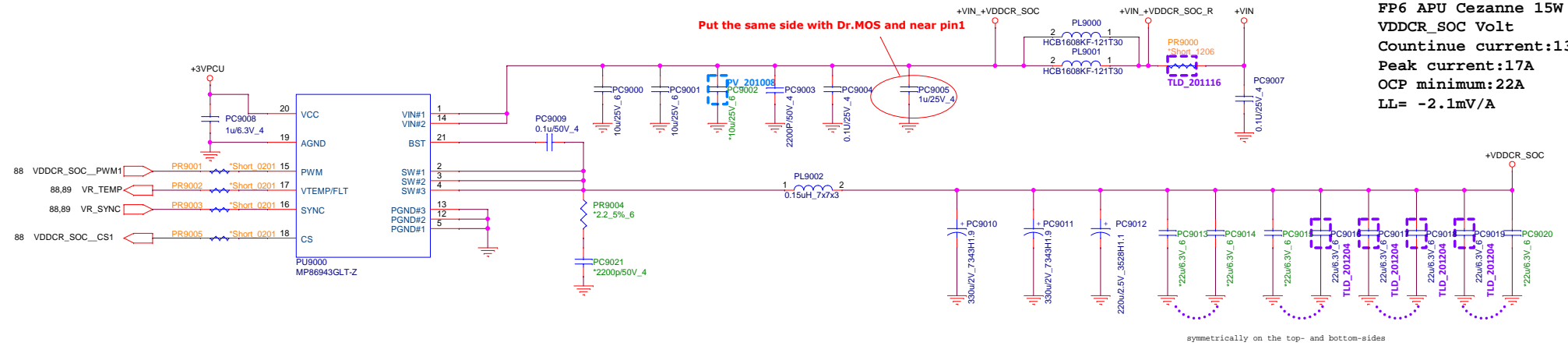







FP6 APU Cezanne 15W  
CPU CORE Volt  
Continue current:40A  
Peak current:90A  
OCP minimum:108A  
LL= -0.7mV/A



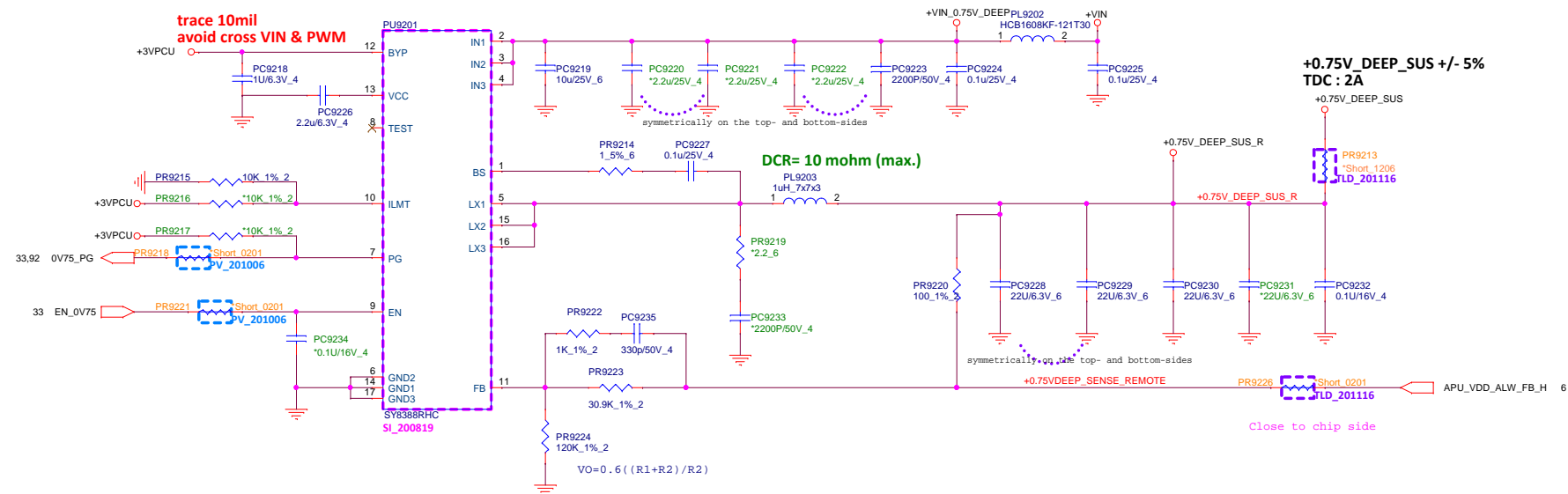
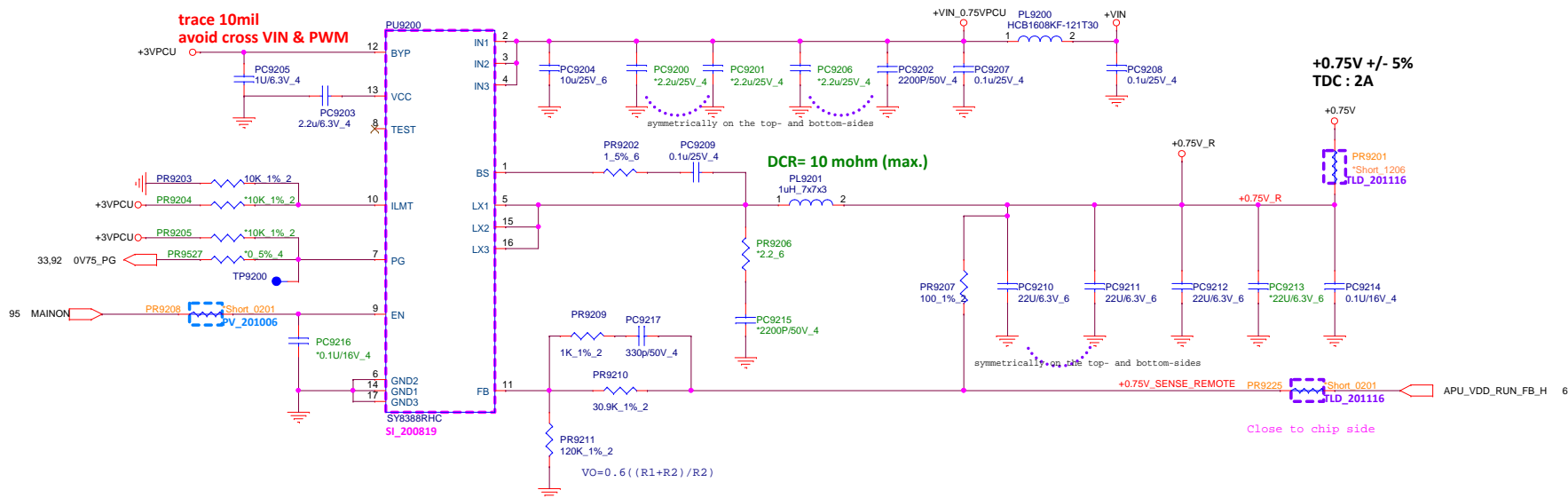


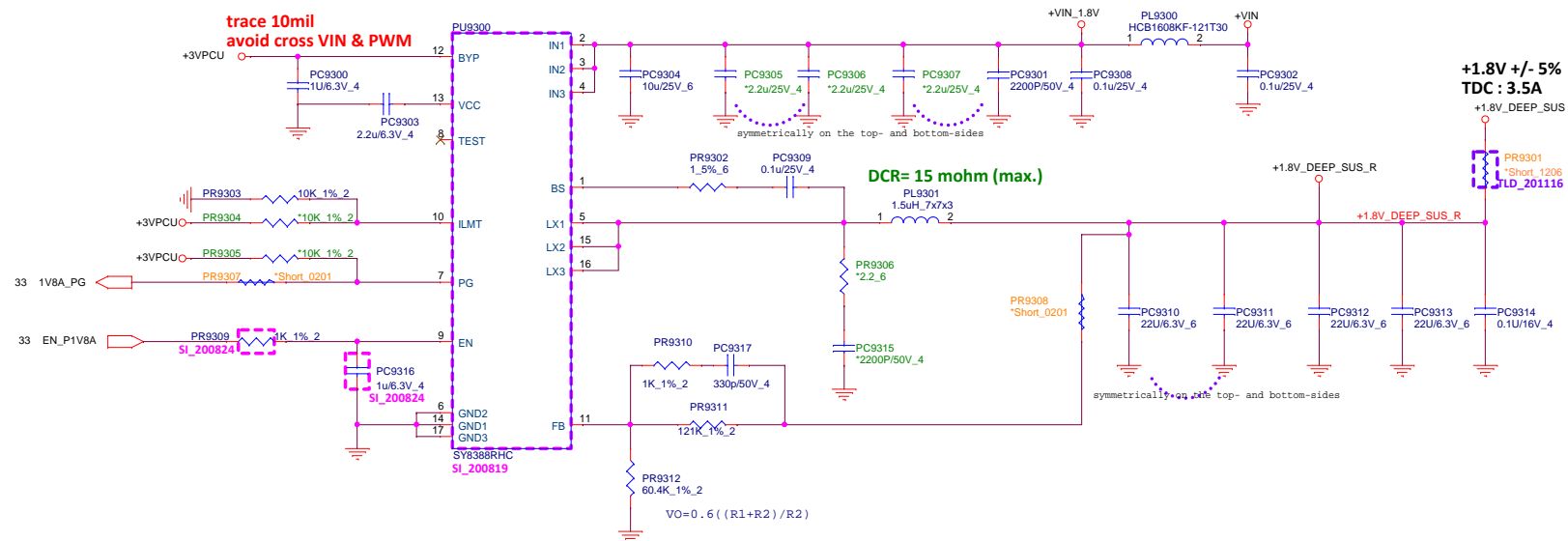


**NB5**  
Custom

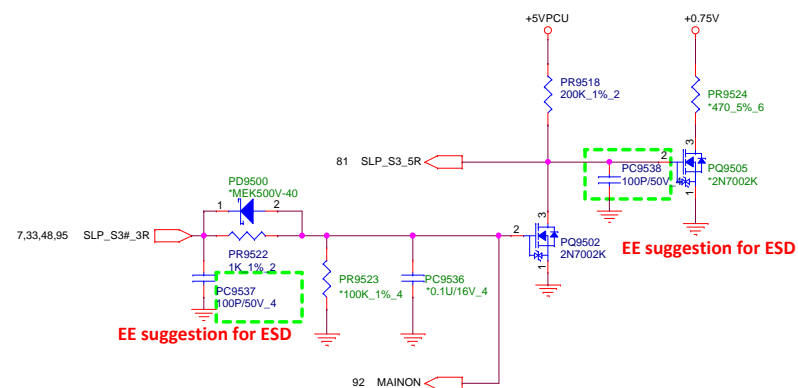
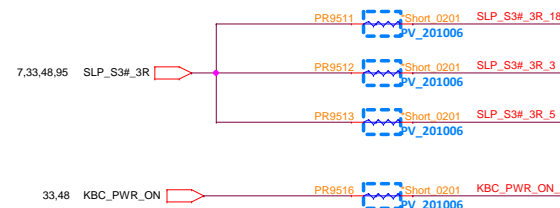
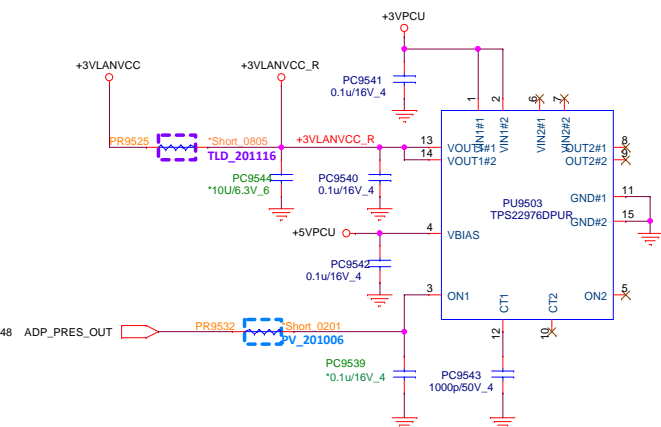
<b>PROJECT : 400 G7 AMD</b> Quanta Computer Inc.		
Size	Document Number	Rev
	<b>CPU POWER</b>	<b>1A</b>
Date:	Monday, December 07, 2020	Sheet 91 of 106








VDDCR\_FCH only for Bristol ridge and Stoney Ridge



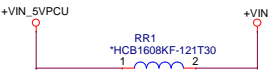
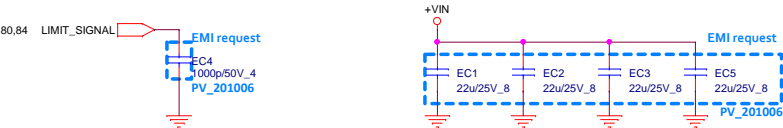



**NB5**  
Custom

<b>PROJECT : 400 G7 AMD</b>		
Quanta Computer Inc.		
Size	Document Number	Rev
	<b>Syatem Load switch</b>	<b>1A</b>
Date:	Monday, December 07, 2020	Sheet 96 of 106

Reserve for EMI & ISEN test

RF Cap






**PROJECT : 400 SERIES**  
Quanta Computer Inc.

Size Custom	Document Number <b>98 -- reserve page(N.A)</b>	Rev 1A
Date: Monday, December 07, 2020		
Sheet 98 of 106		








NB5


**PROJECT : 400 SERIES**  
Quanta Computer Inc.

Size Custom	Document Number <b>A0 -- reserve page</b>	Rev 1A
Date: Monday, December 07, 2020		Sheet 100 of 106



**PROJECT : 400 SERIES**  
Quanta Computer Inc.

Size Custom	Document Number <b>A1 -- reserve page</b>	Rev 1A
Date: Monday, December 07, 2020		
Sheet 101 of 106		



NB5


**PROJECT : 400 SERIES**  
Quanta Computer Inc.

Size Custom	Document Number <b>A2 -- reserve page</b>	Rev 1A
Date: Monday, December 07, 2020		
Sheet 102 of 106		









**PROJECT : 400 SERIES**  
Quanta Computer Inc.

Size Custom	Document Number <b>A6 -- reserve page</b>	Rev 1A
Date: Monday, December 07, 2020		
Sheet 106 of 106		